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NAVAL POSTGRADUATE SCHOOL

Monterey, California



THESIS

EMULATION OF THE AN/UYK-20
TACTICAL DATA COMPUTER
ON THE BURROUGHS D-MACHINE

by

Ralph Harry Anzelmo
and
Theodore Lawrence Kaye

March 1977

Thesis Advisor:

L. V. Rich

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Emulation
of the
AN/UYK-20
Tactical Data Computer
on the
Burroughs D-machine

by

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Submitted in partial fulfillment of the
requirements for the degree of

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NAVAL POSTGRADUATE SCHOOL
MARCH 1977

ABSTRACT

A representation of the Univac AN/UYK-20 computer system has been emulated on the Burroughs D Interpreter-Based System. The entire AN/UYK-20 instruction repertoire has been emulated with the exception of the 'math pac' option (floating point arithmetic and cordic functions), clock and interrupt codes, and input/output operation codes. Modular design with extensive documentation has been implemented throughout program development allowing for ease of modification and further extensions to the existing emulation. Emulation and the hardware architecture of the AN/UYK-20 and the Burroughs D-machine, are discussed in conjunction with the AN/UYK-20 emulation itself. Methods of testing and debugging, sample test programs and recommendations for continued design modifications to the emulation are presented.

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I. INTRODUCTION

A. STATEMENT OF THE PROBLEM

The Navy has been challenged with maintaining the newest, most efficient tactical data systems consistent with the continually increasing demands and requirements of the real-time environment. There is an extensive conversion effort required to change from existing systems to newer more sophisticated technology such as the AN/UYK-20. Inherent in upgrading to a new system is the complex software redesign and modification process which is often hindered by the absence of the new computer system.

Unfortunately, the demands of a military installation require software generation prior to implementation of an upgraded computer system. One solution to this problem is to utilize for software development an intermediate computer system which has the capability of emulating the anticipated target machine. This provides a vehicle for software design, development, and testing prior to transitioning to the new system.

Currently, the Naval Postgraduate School (NPS) Computer Science Department maintains a Burroughs Interpreter-Based System known as the Burroughs D-machine. The D-machine is capable of being microprogrammed to emulate any of a myriad

of target machines. It effectively enables students to create their own computer knowing only the machine instruction repertoire for the control unit in the target machine.

The problem presented was to develop a feasible working model of the AN/UYK-20 on the microprogrammable Burroughs D-machine. The project provided an opportunity to obtain practical experience with contemporary hardware and to manipulate writeable control stores to imitate a Navy tactical computer.

B. APPLICATIONS OF THE AN/UYK-20

The Univac AN/UYK-20 minicomputer is a general purpose militarized digital computer adaptable to numerous tactical applications. The AN/UYK-20 has been successfully utilized in many time-critical, real-time systems including fire control radar, communication controllers, signal processing analyzers for sonar and beacon signals, and numerous weapons control systems. A subsequent chapter will be devoted to the technical aspects and internal design of the AN/UYK-20.

Because of its size, ruggedness, and computing capabilities, the AN/UYK-20 has been designated the Navy's standard tactical minicomputer [1b]. It was selected for emulation in order to provide a feasible platform for software development to those military installations either contemplating or in the process of receiving an AN/UYK-20.

A workable emulation would allow military applications such as data reduction, navigation, telemetry, sensor processing, range tracking and logistics to have software packages developed, tested, and modified prior to arrival of the AN/UUK-20. Furthermore, it would permit personnel to become familiar with the machine by providing advanced training, thereby easing the transition phase to the new system.

C. PROJECT DESIGN OBJECTIVES

Several design techniques were used throughout the development of this project: 1) modularity, 2) structured programming, and 3) extensive documentation. These design features will aid the interested reader as well as simplify any future extensions or modifications to the existing emulation.

Modular design was utilized by creating independent program segments which were individually developed, debugged, and tested. These modules or subroutines provided a strong foundation which were readily modified throughout the entire programming effort. Conceptually, the emulation was divided into relatively small entities which were further reduced to program segments rarely exceeding one page in length.

Structured programming was demonstrated by utilizing a limited number of control flow structures and maintaining a common logical design throughout the entire emulation. Comprehensible code held precedence over extremely efficient

code.

In addition to modularity and structured programming, the entire programming endeavor was supplemented with extensive commenting to provide the necessary self-documentation to promote and facilitate program translation, modification, and fusing with the other independent modules. These concepts promoted the extensive team effort required to achieve the research goals. In addition, it will provide ease of program maintenance and modification in the future.

II. EMULATION

A. HISTORICAL BACKGROUND

The term microprogramming was first utilized in an article by Professor M. V. Wilkes of the Cambridge University Mathematical Laboratory in 1951 [24]. His paper concentrated on a control section within the computer which, when programmatically controlled, performed register-to-register data transfers sequentially and in parallel for the execution of a single machine instruction. A sequence of operations (microinstructions) required for execution of a machine instruction is considered a microprogram.

Traditionally, the computer has been composed of essentially five components: the arithmetic/logic unit, the control unit, memory or storage, input, and output (Figure II-1). The control section sets the proper conditions for the opening and closing of required gates in the logic network. Historically, the control section has been hardware consisting of a series of decoders and flip-flops along with their associated circuitry. Therefore, every machine instruction had a fixed interpretation which was hardwired within the control unit.

In 1957, Wilke's definition of microprogramming was slightly modified. It was defined as a technique of design-

ing the control circuits of an electronic digital computer to interpret and execute a given set of machine operations as an equivalent set of micro-operations [15].

The hardwired control section can be modified by interchanging ROM modules or other hardware components, by replacing the control section with a programmable (dynamically writeable) control store which in itself is a separate word-organized memory (Figure II-2) or by combining both approaches. A programmable control store allows rapid changes in the machine's instruction repertoire while maintaining maximum design flexibility. The resulting computer system is microprogrammable and capable of storing a series of changeable machine personalities.

The computer control store can thus be modified to allow the execution of machine language programs intended for a variety of machine architectures. This process can be compared to replacing hardware components found in conventionally designed computer systems. The primary advantage of microprogrammed logic is the capability to perform various control sequences without hardware modifications. The process through which the hardware components of one machine (host) are made to imitate the specific hardware characteristics of another machine (target) is known as emulation.

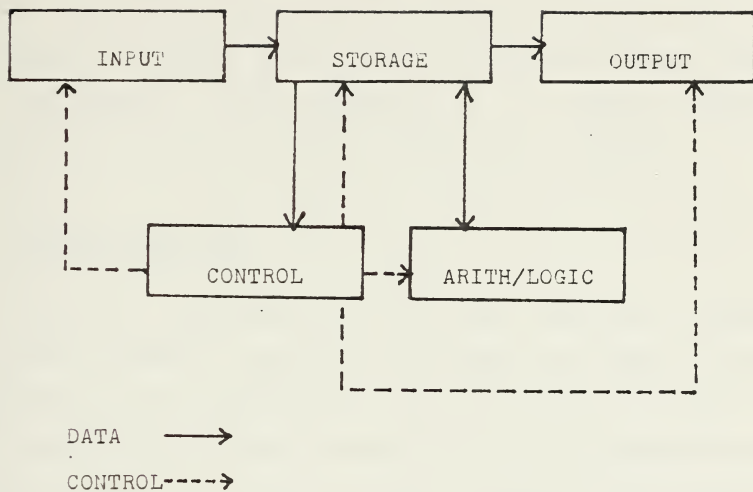


Figure II-1 (11)

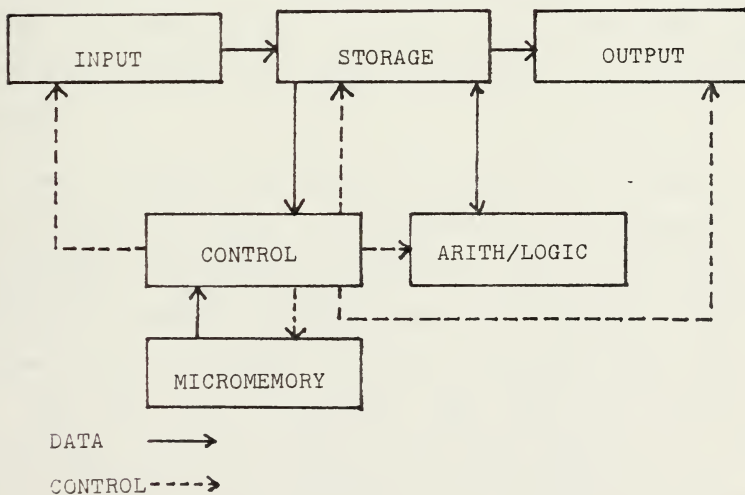


Figure II-2

Emulation allows the computer scientist to create various machine architectures from a single microprogrammable host. The complete set of microprograms (firmware) and the necessary hardware, as well as the required software, added to one computer system enabling it to execute programs designed for another system is known as an emulator.

B. MICROPROGRAMMING

Computer manufacturers have made available numerous microprogrammable machines which permit the user to tailor his instruction repertoire to meet the needs of his particular application. Some examples of microprogrammable computer systems are the Burroughs D-machine, the Nanodata QM-1, the Varian 73, the Standard Logic CASH-8, or the Hewlett-Packard 2100. These microprogrammable systems provide the benefits of flexibility, lower system costs and a systematic approach to system design if utilized effectively.

When a manufacturer designs a dynamically writeable control store, the amount of parallelism to be allowed must be determined. Parallelism is defined to be the simultaneous control of numerous hardware resources. There are basically three forms of control: vertical, horizontal, and residual. In vertical microprogramming, each instruction controls a single operation with program flow being sequential, unless the instruction was a conditional or unconditional branch. By contrast, a horizontally microprogrammed machine is

programmed via instructions which simultaneously control multiple resources including condition testing and microinstruction sequencing.

Horizontal microinstructions usually are not encoded which means each bit controls one machine resource or operation. They usually have a wider word than vertical instructions and consequently consume more memory. Vertical instructions are usually encoded with one or two levels. Encoding means the value of a control field in the microinstruction is a binary code specifying which resource or operation is to be performed. The horizontal microinstructions have the potential of being much more efficient resource managers and consequently are more difficult to optimally design than their vertical counterparts.

Combining the attributes of horizontal and vertical microprogramming results in residual control. This method saves memory by using vertical microinstructions while simultaneously controlling multiple parallel resources via setup registers.

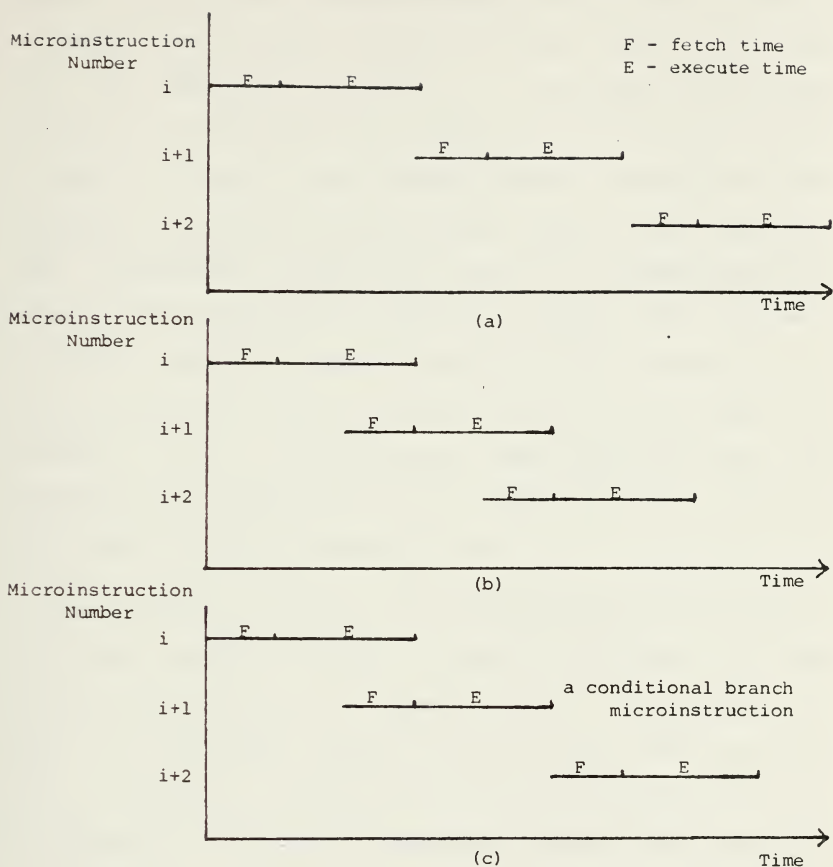
Microinstruction implementation severely effects the speed of microprogram execution. In serial implementation, one microinstruction is fetched and fully executed prior to fetching the next instruction. This technique offers the advantage of logical simplicity while suffering from lack of efficiency since it consumes the maximum amount of time.

'Parallel' implementation permits fetching of the next

instruction before termination of the previous instruction. The obvious advantage is execution speed which is of utmost importance when emulating another machine (Figure II-3) [2].

Another significant microprogramming characteristic is the number of phases used in the execution of each microinstruction. A monophase system means there are no subdivisions of the basic clock pulse and consequently each microinstruction is controlled by the transmission of the leading edge of a clock cycle. In a polyphase implementation scheme, the basic clock cycle is subdivided into minor phases which are independently generated via hardware. Although polyphase operations are more complex and require complicated control, they do permit faster resource manipulation when they are efficiently coded by allowing multiple operations to be performed during the same phase(s).

The microprogrammability of a given computer and the capabilities of its associated microprogramming language are directly effected by the the presence or absence of each of the alternative microprogramming characteristics described above. The microprogramming language spectrum ranges from the lowest level or microlanguage through the assembly languages to the high level procedural languages.



- (a) Serial fetch and execute.
- (b) Parallel fetch and execute.
- (c) Combined serial-parallel where next address depends on conditions in present cycle.

Figure II-3 [2]

The problems of microprogramming can be significantly reduced if suitable software support exists and is readily available. This support is usually in the form of simulators and debuggers. Typically, a simulator provides an alternative to assembly level coding by permitting the user to code in a higher level language and yet achieve the same results at the expense of some added memory and execution time. Debuggers are extremely useful in the developmental stages of microprogramming especially for new and experimental system design. Debuggers permit dynamic access to the machine status and register contents at the instant they are employed, i.e. a trace feature. Some debuggers offer the opportunity of assembling in-line. This option can drastically reduce required debugging time.

The primary application of microprogramming is to implement the necessary control structure required for the analysis and execution of machine level instructions by means of programmed control stores rather than hardwired logic. Therefore, a dynamically microprogrammable computer can provide a software development system which can be a cost-effective approach to experimentation with potential candidates for replacement computer systems or the design of completely new systems to fit the needs of unique applications.

C. THE GOALS OF EMULATION

A well-designed emulation can provide an opportunity to experiment and create software for new computer systems before the actual hardware is available. The utilization of an emulator can almost eliminate reprogramming, consequently smoothing the system transition period. In addition, emulation has provided a workable model of new systems under consideration for procurement, providing a much more detailed cost-benefit analysis of system conversion.

Furthermore, it is often economically sound to emulate a second generation computer with a third generation system. This provides growth to a contemporary system while fulfilling the requirements of the past in a cost-effective manner. However, this can be a disadvantage if the programming staff uses the emulation as a link to the old system and consequently fails to take advantage of the attributes of the new system.

D. EMULATION VERSUS SIMULATION

To accomplish the emulation objectives, certain design features must be incorporated into an emulation. Naturally, execution time and allocated memory are the two foremost considerations. Traditionally, the concept of mimicking another computer has been accomplished by either a simulator or an emulator, two concepts often confused with one another.

A simulator is a series of high level language (HLL) or assembly language statements which individually do not behave like the target machine instructions. The host machine executes its own native instructions in order to imitate the target machine operations. Consequently, simulation is a rather slow technique because it requires an intermediate translation. In addition, simulation of certain instructions such as bit manipulation and shifting operations can require an enormous amount of intermediate code generation demanding a significantly larger memory allocation.

An emulator is a microprogram that is executed on the host machine, performing machine instructions of the target machine. Since an emulator accepts the binary object code of the target machine and directly executes these instructions, it can be extremely efficient in terms of time and space requirements. The execution time of an emulation is dependent upon many factors: clock rates of the two machines, frequency of memory references, high speed shifting compatibility, required register mapping between target and host machines, bit manipulation capability of the two machines, condition code selection and testing, flexible data path selection capability, interrupt similarities, input/output compatibility, and microprogramming efficiency. If the hardware features between target and host machines are extremely compatible and highly efficient microprogramming has been employed, an emulation performance ratio (host

to target) of nearly one to one can be attained. This emulation performance ratio (EPR) has been demonstrated by the emulation of the SKC-2070 on the Nanodata QM-1 computer. It is possible to achieve an EPR better than one to one under ideal situations, when the host machine has a much faster internal operation execution rate [1].

Several distinct advantages can be realized using emulation as compared to simulation. The execution speed is significantly better by at least an order of magnitude. The target machine representation in firmware is closer to the actual hardware design and total access to the lowest machine level is achievable. Perhaps most noteworthy, emulation provides the opportunity to rapidly create test beds for numerous machine architectures and provide a basis for new system development.

E. EMULATION TECHNIQUES

Traditionally, there have been three approaches for emulating machine instructions: 1) hardware or firmware assistance to a software simulation as demonstrated by the IBM 360/b5 emulation of the IBM 7090, 2) independent host system hardware or firmware which provides for complete execution of the target machine's instruction repertoire of which the Burroughs D-machine emulation of the AN/UYK-20 is an example, and 3) an auxiliary processor which is operated in conjunction with the host machine to execute target machine instructions [14].

Software-controlled emulation is usually characterized by categorizing the target machine instructions into three distinct classes: easily emulated instructions, complex instructions not readily emulated, and those instructions not deemed necessary for the desired application. Instruction usage is significant in this classification process. Each class of instructions becomes a candidate for direct hardware or firmware implementation. The first emulated function in this approach is usually the fetch and analysis operation. After the instruction is analyzed, the appropriate opcode subfunction can be executed.

An alternative emulation technique is the firmware-controlled method. This approach is identified by having system control reside completely in firmware or hardware during the emulation process. All instructions are executed on the host machine as if they were indigenous to the target machine. This method is much more efficient than the software-controlled technique; however, it is more expensive and the cost differential is directly related to the required performance level. Performance is dependent upon the number of required data paths, arithmetic units, and other additional logic circuitry which must supplement the host machine architecture.

Upon entering the emulation mode in a firmware-controlled emulator, the machine performs like the target machine until encountering an exit situation. There exists three exit modes: 1) priority interrupt, 2) not implemented

instruction, and 3) deliberate exit because of a debugging routine.

The third emulation technique consists of utilizing auxiliary hardware electronically attached to the host computer for the sole purpose of executing target machine instructions. In effect, a target machine is composed of host machine hardware with the necessary additional components required to create an effective emulator.

F. EMULATION HARDWARE

The development of writeable control stores and microprogramming techniques have significantly influenced computer design. This section will describe some of the available dynamically microprogrammable hardware (Figure II-4).

The Hewlett-Packard 2100 is a general purpose minicomputer. It has a unique control store divided into two segments. One section is ROM and the other section is user programmable. The machine is vertically microprogrammed using a standard 80 instruction machine language repertoire. A debugger and assembler assist the user in microprogram development [2].

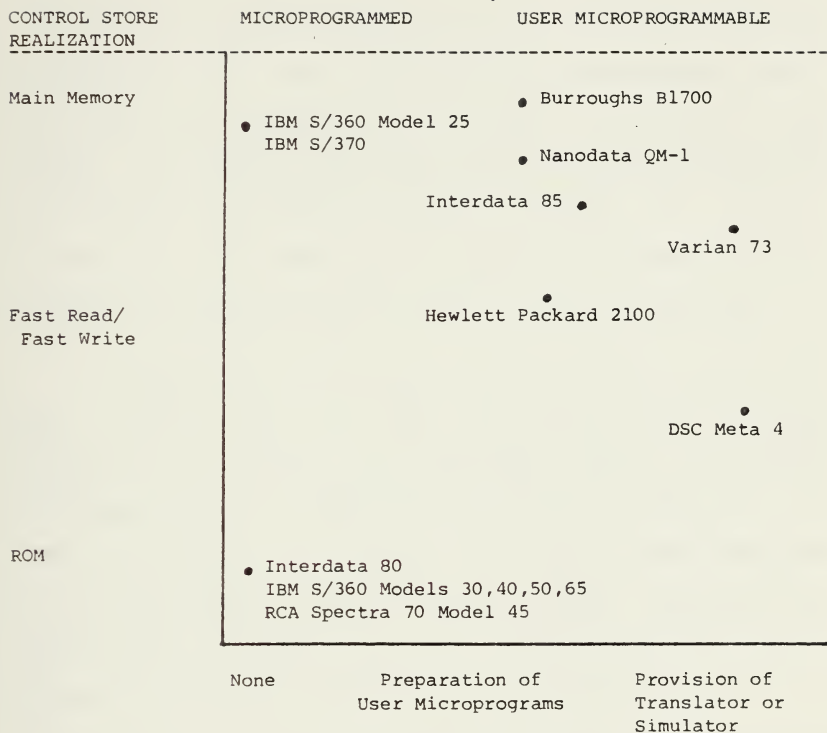
The Standard Logic CASH-8 is a high speed digital controller with a separate control store. It consists of 16 general purpose registers and an accumulator. The CASH-8 is vertically microprogrammed but does not support any language

above microlanguage [2].

The Varian 73 is a general purpose minicomputer that has a 150 instruction set. The horizontal microinstruction consists of 64 bits with 25 fields, some of which indicate register transfers, ALU operations, shifting, control store addressing, condition testing, I/O control and memory operations. The Varian 73 contains both a ROM control store and a writeable control store loadable from main memory. A microprogram assembler and interactive simulator are available [2].

The Nanodata QM-1 is unique in that it contains both a control store and a nanostore which are both loaded under user program control. The 18-bit vertical microinstructions are stored in the control store, fetched and then interpreted under nanoprogram control. A horizontal nanoinstruction is 360 bits which is subdivided into five 72-bit vectors. Assemblers for both microprograms and nanoprograms are available [2].

The previously described machines represent a small sample of the available microprogrammable computer architectures. The availability and flexibility of these computer systems has stimulated demand for these devices. Consequently, hardware manufacturers have been compelled to produce writeable control store equipment to satiate the needs of the computer market.



SUPPORT AVAILABLE TO USERS

Note: Relative microprogrammability is the distance from the origin to the machine point in two space.

Figure II-4 [2]

III. AN/UYK-20 ARCHITECTURE

Constructing an efficient emulation requires a precise understanding of the architecture and performance characteristics of the machine being emulated. An emulation must attempt to match the target machine's features and maintain its flexibility of hardware design as closely as possible. Although it is not required, an operational demonstration of the emulated machine can solve many emulation questions.

In emulating the AN/UYK-20, architecture and performance criteria were derived from technical publications, since an actual machine was unavailable. When inconsistencies appeared in the documentation, specific questions were posed to a UNIVAC field engineer, who often tested programs on the AN/UYK-20 to resolve inconsistencies. Documentation coupled with an expert consultant provided sufficient information for emulating the AN/UYK-20 successfully.

The intent of this chapter is to outline those features of the AN/UYK-20 significant to the emulation. A detailed hardware description can be found in Refs. 20, 22, 28.

A. HARDWARE DESIGN

The AN/UYK-20 was designed for the Navy to fulfill the requirements for small or medium size general purpose data processing in shipboard, mobile shelter, or other military environments. Sperry Univac incorporated minicomputer technology in constructing the AN/UYK-20, including MSI circuitry design, microprogrammed control, memory modularity, and asynchronous or synchronous input/output channels.

The AN/UYK-20 had to be extremely flexible in its applications, offering a wide range of configuration possibilities which were derivatives of the basic design. Modularity, a concept highly desirable in a military environment, was achieved by offering options that could be easily added using printed circuit cards and/or memory modules.

The AN/UYK-20 can accommodate up to eight 8K, sixteen-bit word boards of magnetic core storage with an access time of 750 nanoseconds. The central processor is controlled by a programmable micromemory which can be expanded by an additional 512 words. The microprogram controller is programmed at the factory, but the additional micromemory option is user defined. Both sections of micromemory are programmed using fusible links, and once programmed they are completely static (Figure III-1).

A memory interface is responsible for the transfer of data to memory from the central processor (CP) and input/output controller (IOC). Both the IOC and the CP are

capable of accessing all of memory (65,536 words maximum). The addition of direct memory access (DMA) provides a second memory interface and an additional access port which is connected to each of the two 32K memory segments.

The input/output controller permits the central processor to communicate with the external devices without interfering with program execution. The IOC has a maximum of 16 parallel or serial channels. Parallel data transfer takes place asynchronously using 8-bit, 16-bit, or 32-bit transfers. Serial interfaces are either synchronous or asynchronous, with word-to-serial or serial-to-word conversions occurring in the IOC. The IOC and CP compete for memory access through the memory interface with priority given to the IOC in the event of a simultaneous request. The IOC is permanently assigned several memory addresses for command word and interrupt word storage.

The addressable high-speed registers available in the AN/UYK-20 include the program address register (P-register), two 16-bit status registers (SR1 and SR2), a real-time clock register (32-bits), a monitor clock register (16-bits), and a set of sixteen 16-bit general registers. An additional stack of 16 general registers is an available hardware option.

The sixteen general registers were included to enhance the speed and performance of the AN/UYK-20, allowing most programs to use a great proportion of register-to-register

instructions. These general registers can be used as accumulators for arithmetic, shift, or logical functions, as index registers, or as temporary storage locations. The second set of general registers can be readily employed via a status bit. This status bit designates which general register stack is to be utilized. The duplicate set of general registers yields dividends in a multi-task or heavy-interrupt processing environment. This additional register set can be used to provide high-speed temporary storage, thus avoiding slower main memory storage of working variables.

The two 16-bit status registers and the program address register represent the machine status of the AN/UYK-20. When these registers are collectively referenced, they are called the program status word (48-bit PSW). The P-register indicates the next instruction to be executed. This instruction may be a 16-bit single-word instruction or a 32-bit double-word instruction. Program control can be modified by using an instruction which manipulates the contents of the P-register.

Status register 1 contains bit information concerning condition code settings, overflow, and carry bits, interrupt codes, and numerous other machine indications (Figure III-2).

AN/UYK-20 FUNCTIONAL ARCHITECTURE

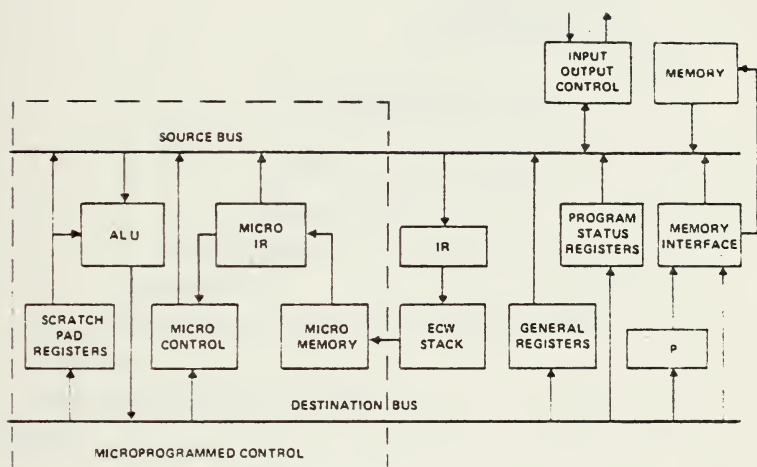
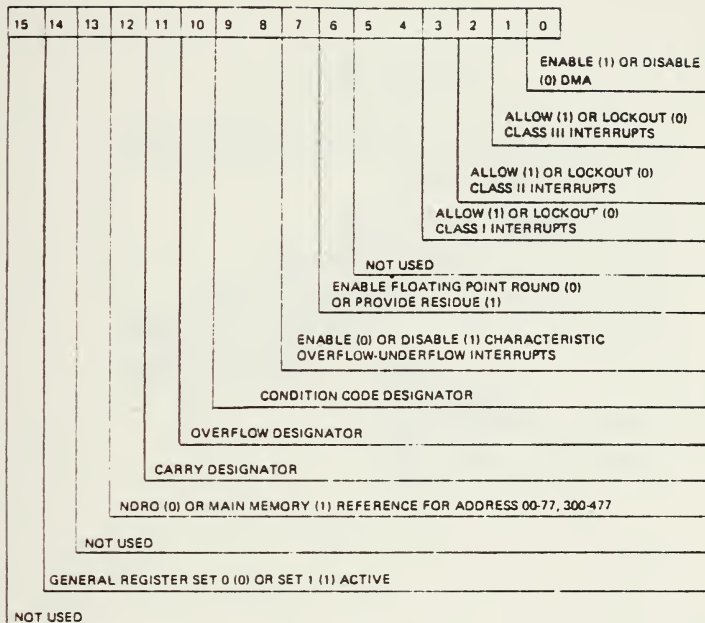


Figure III-1 [22]

STATUS REGISTER 1



CONDITION CODES

SR BITS 8 and 9	ARITHMETIC	COMPARE
00	0	$(R_a) = (R_m)$ or (Y)
01	>0 (POS)	$(R_a) > (R_m)$ or (Y)
10	Not Used	Not Used
11	<0 (NEG)	$(R_a) < (R_m)$ or (Y)

Figure III-2 [23]

Status register 2 holds control bits for direct or indirect addressing, and holds interrupt codes. Interrupt processing routines set bits in the interrupt code field corresponding to the IOC interrupt (Figure III-3).

STATUS REGISTER 2

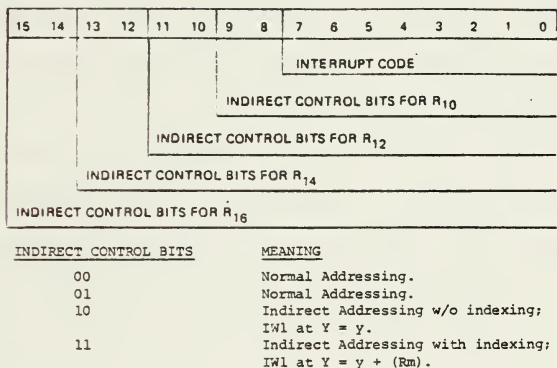


Figure III-3 (23)

The real-time clock and monitor clock registers provide program-controlled interrupt capability which is useful for timing and synchronizing program segments with real-time events. The real-time clock (RTC) is a 32-bit register used as count-up storage while the monitor clock (MON) is a 16-bit count-down register. A one kHz internal oscillator controls the counting speed of both registers. An optional

external clock operating at a frequency up to 50 kHz is also available.

Interrupt processing in the AN/UUK-20 is conducted using a priority level scheme which classifies interrupts into three priority levels (classes). Interrupts within the same class are assigned a priority ranking and a code which identifies which processing routine to execute. During interrupt handling, all interrupts of the same level or lower level are locked out until the CP is completed processing the current interrupt. Higher priority interrupts can override the lockout and cause the CP to honor them first, holding the lower level interrupts in abeyance until higher level interrupt processing is completed. The highest priority interrupts are hardware malfunctions, followed by software interrupts, and at the lowest level, IOC interrupts.

Permanent locations in memory corresponding to each interrupt class hold the PSW and RTC when an interrupt is being honored. Likewise, other permanent memory addresses assigned to each interrupt class hold the appropriate interrupt routine entrance location to be loaded into the PSW.

Memory addressing is accomplished using 64 page address registers which separate memory into 1024-word pages. Absolute addresses are formed by isolating the upper six bits of the relative address to find the page address register number, and then concatenating the lower six bits of the

page address register contents with the lower ten bits of the relative address (Figure III-4). Any operation that stores into memory sets the most significant bit of the page address register used in generating the address.

Some additional hardware features of the AN/UYK-20 are those functions available on the maintenance panel of the machine itself. These include a breakpoint feature which allows an operator to insert from the panel an address which causes the AN/UYK-20 to stop execution when the selected address is referenced. Other available toggles allow halting execution programmatically using Key 1 or Key 2 on the maintenance panel. These additional hardware features are useful debugging tools.

MEMORY ADDRESS GENERATION

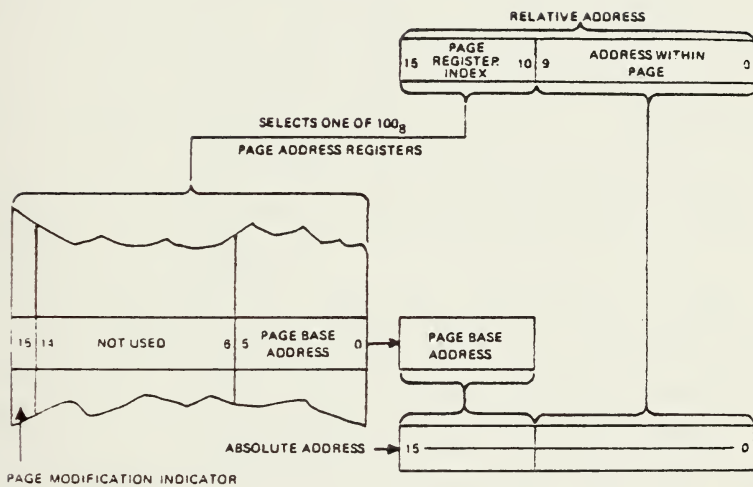


Figure III-4 [22]

B. INSTRUCTION FORMATS AND REPERTOIRE

1. Repertoire of Instructions

The AN/UYK-20 instruction set is composed of nearly 260 separate instructions designed to be both versatile and comprehensive. Both single-word (16-bit) and double-word (32-bit) instructions are available. Some of these instructions are specifically designed to meet the requirements of a real-time environment. A few sample instructions include:

- a. Local jump - used to facilitate loops, saving several steps in program execution.
- b. Reverse register - used in a communication environment when data is received in one sequence but must be transmitted in reverse sequence.
- c. Set bit, clear bit, and test bit - used to test individual bits in registers saving considerable execution time in programs that communicate via flags and status words.

Additional flexibility is provided when the 'math pac' hardware option is included in the AN/UYK-20 configuration. Some 33 additional opcodes are added to the instruction set in order to increase the computational capabilities of the machine. An instruction for square root, double precision multiply/divide instructions, as well as hardware trigonometric and hyperbolic functions which utilize coordinate conversion algorithms (cordic) are included.

Single-word instructions are generally employed when manipulating operands in high-speed registers. Double-word instructions are used in operations involving direct or indirect addressing with or without indexing, or supplying 16-bit constants to programs. Typical instruction speeds for a single-word versus a double-word instruction are:

	SINGLE-WORD	DOUBLE-WORD
ADD	.75 - 1.5 usec	1.5 - 2.25 usec
LOAD	.75 - 1.5 usec	1.5 - 2.25 usec
MULTIPLY	3.8 - 4.0 usec	4.4 - 4.6 usec
DIVIDE	6.8 - 7.0 usec	7.4 - 7.5 usec

Nearly all instructions affect condition bits in status register 1. The AN/UYK-20 sets these bits as a result of two types of operations. Most instructions that do not involve compare logic are categorized as arithmetic instructions. When the result of the arithmetic operation is determined and is about to be stored in memory or a register, a condition code is set indicating whether the result is positive, negative, or zero. Compare instructions set the condition bits based on a greater than, less than, or equal to comparison of two registers or a register and the contents of a memory address.

Two other bits in SR1 are set as a result of computational or shifting instructions. The overflow designator is set whenever an arithmetic or shift operation requires more bits than are provided for in a register (16 bits).

The carry designator is set when an arithmetic operator generates a carry beyond the most significant bit of the register.

The AN/UYK-20 allows five different types of operand formats: single-length, byte, literal, optional floating point, and double-length. Single-length operands are 16-bit values with the sign bit assumed to be in the most significant bit. In arithmetic calculations, the single-length word is assumed to be a two's complement integer. Byte operands are considered 8-bit unsigned integers, and can be the most significant or least significant half-word of a memory location. Literal operands are 4-bit unsigned integers denoted by the 'm' field of a literal type instruction. Floating point operands are formed using two adjacent registers or memory locations with fields containing the sign of the fraction, the characteristic, and 24 bits of the fraction.

Double-length operands are concatenated from two adjacent registers or two adjacent memory addresses. The most significant half of the double-length operand is contained in the low-order register or memory address, and the least significant half in the next sequential register or address. The sign bit for both words resides in the high-order bit position of the most significant half-word and when used in an arithmetic calculation, the double-length operand is treated as a two's complement integer. Instructions involving double-length operands require the low-order

register or memory address to be even, since the adjacent cell address is formed by 'OR'-ing a 1 in the least significant bit of the address.

2. Instruction Format

The AN/UYK-20 has five different instruction word formats, designated by two-letter mnemonic codes. These codes are: RR (Register-Register), RL (Register-Literal), RI (Register-Immediate), RK (Register-Constant), and RX (Register-Index). Each of these formats are designated in the instruction word by a combination of the opcode field and the subfunction code. Registers are identified in the 'a' and 'm' fields of the instruction, and are referred to by the notation Ra and Rm. The 'v' field is treated as an address or arithmetic constant, depending on the instruction (Figure III-5).

The format RR single-word instructions perform operations involving the registers specified by the 'a' and 'm' fields. No memory references are made to access operands, causing considerable savings in execution time. The 'a' or 'm' field may be used to index special operations on registers.

Format RL instructions use a 16-bit instruction word, using one or two general registers. The 'a' designator selects the general register Ra or register pair Ra, Ra + 1. The 'm' designator contains the 4-bit literal value which will be used in the instruction.

INSTRUCTION FORMATS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RR	Op*				U		a				m					

a selects R_a ; m selects R_m .

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RL	Op*				U		a				m					

a selects R_a ; m contains 4-bit constants.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RI-1 Local Jump	Op*				1		d									

d is signed number of instructions to jump, relative to current position.
(+ is forward; - is backward)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RI-2 Indexed Memory	Op*				1		a				m					

a selects R_a ; m selects R_m . R_m selects memory address.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
RK	Op*							2		a							m																						
																	y																						

a selects R_a ; $m \neq 0$ selects R_m , $m = 0$ selects 0.
Operand = $y + R_m$ or 0.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX	Op*				3		a				m						y															

a selects R_a ; $m \neq 0$ selects R_m , $m = 0$ selects 0.
 $y + R_m$ or 0 selects memory address.

*Op is operation code

Figure III-5 [23]

RI format single-word instructions are separated into two categories. RI Type 1 instructions are local jump instructions where the P-register is increased or decreased by the 'd' field in the instruction. The 'd' field represents the two's complement deviation value and allows the P-register to be altered a maximum of +177 octal or -200 octal. RI Type 2 instructions involve operations that use the general registers Ra and Rm, and a memory address specified by the contents of Rm.

The format RK instructions contain 32 bits of information. The upper 16-bits contain the operation code and the designator fields. The 'a' field selects the general register Ra, and the 'm' field denotes how the next word, containing 'y', is to be used. If 'm' equals zero, then the effective operand address Y, equals 'y'. If 'm' does not equal zero, then Y is formed by adding the contents of Rm to 'y'.

Format RX are double-word instructions similar to the RK instruction that use direct and indirect addressing techniques determined by the 'm' field. If the 'm' field equals zero, then direct addressing without indexing is employed, with the effective operand address formed from the 'y' field itself. If the 'm' field equals 1 through 7, 11, 13, 15, or 17 (octal), then direct addressing with indexing is employed. The effective operand address is formed by adding the contents of Rm to 'y'. An 'm' field value of 10, 12, 14, or 16 (octal) indicates indirection is to be

employed, and the indirect address control fields in status register 2 contain information which is used to generate the effective operand address or a pair of indirect words. When the control fields equal 0 or 1, then direct addressing with indexing results. If the control field equals 2, then the contents of the first indirect word (IW1) is located at 'y'. Finally, if the control field equals 3, then IW1 is located at 'y' indexed by the contents of Rm. Indirect word format is shown in Figure III-6. Cascaded indirection is possible provided that the indirect words are properly encoded.

Byte addressing is accomplished using RX format instructions. A byte identifier (B) is used to determine which half-word (8-bit) is to be referenced. If B equals 0, then the most significant half-word in address Y is the operand byte. If B equals 1, then the least significant byte at Y is the operand. The least significant bit in the indexing register is used as the byte identifier, and the remaining 15 bits are used as the indexing value for finding Y. Indirect byte operand addressing formulae are included in Figure III-6. The following formulae apply for direct byte operand addressing:

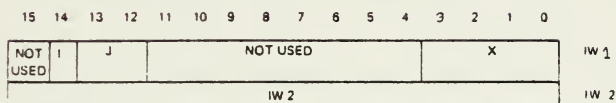
$$m=0, Y=y, \text{ and } B=0$$

$$m=1-7, 11, 13, 15, \text{ or } 17 \text{ octal}$$

$$Y=y + (Rm)/2 \text{ and } B=\text{LSB of } (Rm)$$

The preceding section has described the fundamentals of the AN/UYK-20 instruction formats. References 21 and 23 should be consulted for further information concerning instruction formats and decoding.

INDIRECT WORD FORMATS



OCTAL J VALUE	ADDRESS DETERMINATION
0	$Y = IW2$; if byte mode, upper byte is used.
1	$Y = IW2 + (Rx)$; if byte mode, LSB of R_x determines byte. *
2	$Y = IW2 + (Rm)$; if byte mode, LSB of R_m determines byte. *
3	$Y = IW2 + (Rm+1)$; if byte mode, LSB of $Rm+1$ determines byte. *

I = 0, DIRECT ADDRESSING, OPERAND AT ADDRESS Y

I = 1, CASCADED INDIRECT ADDRESSING, NEW INDIRECT WORD 1 AT ADDRESS Y

* To determine the operand address when in byte mode, the contents of R_x , or R_m , or $R_m + 1$ are right shifted 1 bit position and zero filled in the left most position

Figure III-6 (23)

IV. BURROUGHS D-MACHINE

A. HARDWARE DESCRIPTION

The microprogramming facility at the Naval Postgraduate School is composed of a Burroughs Interpreter-Based system. This system possesses the characteristic of being dynamically microprogrammable and is designed using a simple building block structure. A typical system is made up of a number of interpreters (processors), main memory modules, and input/output devices, along with a switch interlock device (SWI) controlling data flow on the data bus connecting the interpreters to main memory and peripheral devices. The heart of the system is the interpreter, also referred to as the D-machine.

A D-machine possesses five functional modules: the logic unit (LU), the control unit (CU), the memory unit (MU), nanomemory (NM), and microprogram memory (MPM). The system presently installed in the Computer Science Department combines nanomemory and microprogram memory into one functional unit. The architecture of the D-machine is designed around 8-bit word slices. Word lengths from 8 bits to 64 bits are permissible using the same functional unit (Figure IV-1).

INTERPRETER BLOCK DIAGRAM

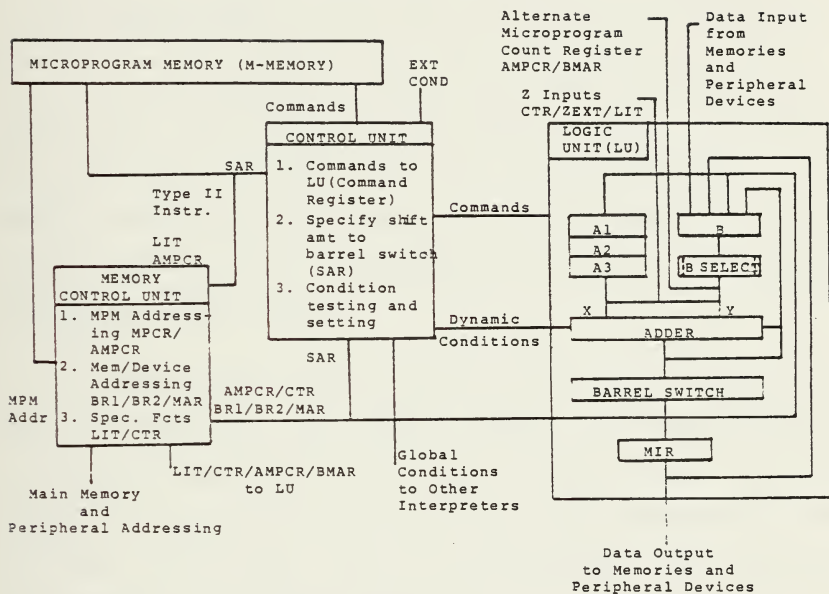


Figure IV-1 (a)

The D-machine used for this thesis has been configured as a 32-bit word processor. Reference 17 provides a thorough and concise description of the architecture of an interpreter-based microprogramming system. Reference 6 details the specifics of D-machine microprogramming which must be thoroughly understood by the programmer.

1. Logic Unit

The D-machine's logic unit performs shifting, arithmetic, and logic functions and contains scratch pad registers and data interfaces for the switch interlock. All adder operations are performed using two's complement arithmetic, and shifting is accomplished in a matrix of gates called the barrel switch.

The scratch pad registers A1, A2, and A3 are identical in function. They act as temporary storage registers within the D-machine and serve as primary inputs to the adder. The control unit determines which register will be an input to the adder. Any of the A-registers can receive the output from the barrel switch.

The B register functions as the primary external input interface from the switch interlock. It acts as the second input to the adder and can receive certain direct inputs from the adder's arithmetic operations. The b register can be loaded from any of the following sources:

- a. The barrel switch output.
- b. The adder output.
- c. External data from the switch interlock (or control panel switches).
- d. The memory information register (MIR).
- e. The complements of four bit or eight bit carries.
- f. The barrel switch ORed with the adder, external data from the switch interlock, or MIR.

The output of the B register is filtered prior to gating into the adder. The 'filter' consists of true/complement selection gates which are divided into three sections: the most significant bit, the least significant bit, and all the remaining central bits. The output of this filter is the independent result of these sections and may be either all zeroes, all ones, or the true contents or one's complement of the contents of the respective bits of the B register.

The memory information register is the interface to the switch interlock. MIR functions as a buffer to main memory or to a peripheral device. It is an output destination of the barrel switch and its output can be sent to the B-register or the switch interlock.

The adder in the logic unit performs all arithmetic functions and can be categorized as a version of a carry look-ahead adder. The control unit can gate various combi-

nations of A, B, and Z inputs to the adder. An 'A' input is defined as an input from one of the three scratch pad registers. A 'B' input is the output of the B register's true/complement filter gates. A 'Z' input is an external input to the logic unit and can originate from one of the following sources:

- a. The output of the counter in the memory control unit (MCU) which is gated to the most significant eight bits of the adder with the remaining bits zeroed.
- b. The output of the literal register in the MCU which is gated to the least significant eight bits of the adder with the remaining bits zeroed.
- c. An optional input which is gated into the middle bytes of the adder with the most and least significant bytes zeroed.
- d. The output of the alternate microprogram count register (AMPCTR) in the MCU which is gated into the least significant 12 bits of the adder (13 bits for 8K micromemory machines) with all other bits being zeroed.
- e. All zeroes.

Two inputs, selected from the A, B, or Z sources, are always gated to the adder. These inputs are referred to as X-select and Y-select. An X-select input may be either an A input or a Z input. If it is not specified, it is

assumed to be zero. A valid Y-select has either a B, Z or 1 as its input. Some Z inputs, however, are valid only as Y-select inputs. Any combination of valid X-selects and Y-selects are permissible addends, with an option of adding a one to the least significant bit. For subtraction operations, the value to be subtracted must be a Y-select; the Y-select input is subsequently two's complemented and gated to the adder. All binary Boolean operations between two adder inputs are allowed, and dynamic condition bits for overflow (AOV), all bits true (ABT), and most/least significant bit test (MST/LST) are available to the control unit for testing. Bit testing is a valuable feature for decoding instruction words.

The barrel switch is a matrix of gates that accepts parallel data from the adder and shifts the data any number of places to the left or right with zero fill. It also can right shift the word in an end-around fashion. The output of the barrel switch may be directed to any of the following destinations simultaneously:

- a. The A registers.
- b. The B register.
- c. The memory information register.
- d. The least significant 16 bits to the MCU registers.
- e. The least significant three to six bits to the control unit shift amount register (bit length depending on the word size of machine).

2. The Control Unit

The control unit has five major sections: the shift amount register (SAR), the condition register (COND), part of the control register (CR), the decoder for microprogram memory content, and clock control. This module of the D-machine manages the functions of the processor, and is directly responsible for logic unit operation.

SAR and its associated logic control shifting operations by loading shift amounts into SAR and generating the required controls indicated by the current microinstruction for the barrel switch. In addition, the SAR's logic generates the 'word length complement' of the SAR contents where the complement is defined to be that amount which would restore the bits of a word to their original position after an end-around shift of N followed by an end-around shift of the 'complement' of N. For example, if an end-around right shift of 20 was required in a 32-bit D-machine, another end-around shift of the complement of 20 (12) would be required to restore the contents to its original value.

The condition register has four major functions:

- a. It stores 12 resettable bits which are used as error indicators, interrupts, status, and lockout indicators.
- b. It selects one of 16 condition bits for performing conditional operations. These 16 bits are composed of the 12 condition bits of the

condition register plus the 4 dynamic conditions generated by the LU adder during the present clock time.

- c. It decodes bits from the memory for resetting, setting, or requesting the setting of designated bits of the condition register.
- d. It resolves priority between interpreters in the setting of global condition bits (GC), thereby providing a method of controlling inter-
interpreter lockout.

The control register stores the control bits of the 56-bit microinstruction that are not being used in the first phase of the execution cycle. The control register is subdivided into sections which are used by the memory control unit, the logic unit, and the control unit during the execution phase of a microinstruction. For a description of timing and phases, see section C of this chapter.

3. Memory Control Unit

The memory control unit provides the basic addressing interface between the D-machine and both main memory (S-memory) and microprogram memory (M-memory). One MCU can address 64K words (256K bytes) of main memory, and if the D-machine is configured with a second MCU, a maximum of 128K words can be addressed.

The memory control unit has three major sections:

- a. The microprogram address section controls the addressing of microprogram memory and the sequencing of microinstructions. It contains the microprogram count register (MPCR), the alternate microprogram count register (AMPCR), the incrementer, the microprogram address controls register, and their associated logic. For standard 4K M-memories, the MPCR and AMPCR are 12 bits long. For 8K M-memories, MPCR and AMPCR are 13 bits in length (the D-machines installed at the Postgraduate School employ 8K M-memories). AMPCR is a Y-select input to the logic unit adder.
- b. The memory/device address section contains the 8-bit memory address register (MAR), two 16-bit base registers (BR1 and BR2), output selection gates, and associated control logic. When forming a memory address, the lower eight bits of a base register and MAR are concatenated. The concatenated 24-bit contents of BR1/ BR2 and MAR (BMAR) is a valid Y-select input to the logic unit adder.
- c. The Z register section contains two registers which are Z inputs to the logic unit adder. The literal register (LIT) is an 8-bit register into which constants are loaded. An 8-bit counter (CTR) is used in conjunction with a counter overflow condition bit to control iterative

looping. The Z register section also contains selection gates for the loadable counter and its associated logic.

4. Microprogram memory (M-memory)

A D-machine may have a dual or single microprogram memory scheme. As indicated earlier, the D-machines used in this emulation project had a single microprogram memory, consolidating the microprogram memory and nanomemory into one 56-bit programmable store memory, often referred to as M-memory. Microprograms, consisting of 56-bit microinstructions, are dynamically changeable by the user, thus distinguishing the D-machine as an extremely flexible computing device.

The sequencing of microprogram instructions is controlled by a condition bit procedure which determines the successor command to be executed. M-memory provides data to the condition testing logic which then determines which condition is to be tested. The output of the condition testing logic is a true/false signal that is gated to the successor selection logic. This logic then selects between the three true and three false successor bits also provided by the M-memory word. The three selected bits provide eight possible successor combinations:

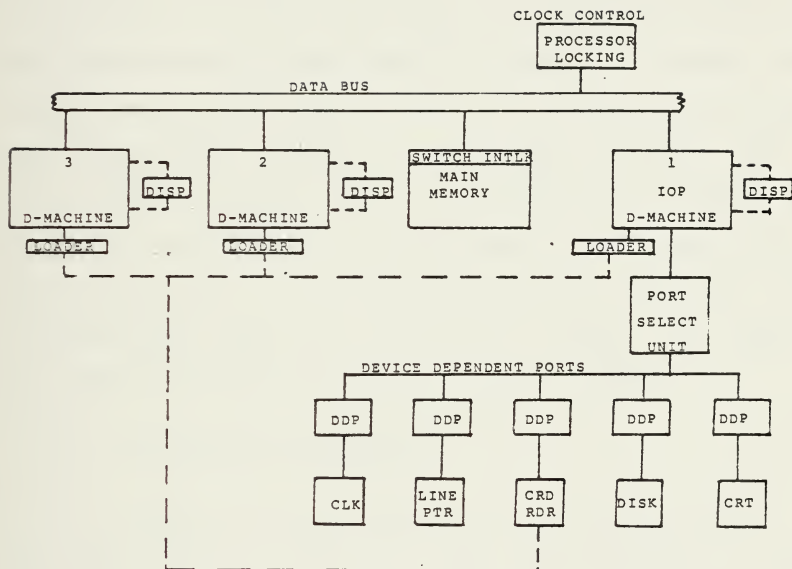
- a. WAIT Repeat the current instruction.
- b. STEP Step to the next instruction.
- c. SKIP Skip the next instruction.
- d. JUMP Jump to another M-memory address.
- e. RETN Return from a microprogram subroutine.
- f. CALL Call a microprogram subroutine.
- g. SAVE Step and save the instruction address.
- h. EXEC Execute one instruction out of sequence.

The particular successor command chosen controls gates which select the appropriate M-address from MPCR or AMPCR and provides incrementing logic for generating the next M-memory address. Except for the EXEC command, the MPCR is loaded with this M-memory address.

B. NPS MICROPROGRAMMING FACILITY

1. Physical Description

The Computer Science Department of the Naval Postgraduate School possesses a Burroughs Interpreter-Based System consisting of three interpreters (processors) also known as D-machines, a 64K 32-bit word, main memory module, a card reader, a dual cartridge disk drive, a line printer, and a Datamedia 2500 CRT functioning as a supervisor's console (Figure IV-2). All input and output is performed through a single D-machine processor, hardware configured with device dependent ports (DDP) for peripherals and the external clock.



NAVAL POSTGRADUATE SCHOOL MICROPROGRAMMING FACILITY
BURROUGHS INTERPRETER-BASED SYSTEM

Figure IV-2

After initial light-off and bootstrap, the system is configured into two Burroughs 6700 - LIFO ALGOL Stack-machines, each addressing 32K of memory and each communicating with the input output processor (IOP) in a pseudo-multiprocessing environment. Software, written in ALGOL, is provided which runs on the B-6700 system. A resident monitor control program and disk file manager control the maintenance of system files and the execution of jobs in a batch environment. Both D-machines compete for system jobs input from the card reader or CRT. Other software available includes an ALGOL compiler (a derivative of ALGOL 60), a microprogram translator called TRANSLANG, a line editor, and a simulation program for microprograms. TRANSLANG provides the medium by which microprograms are written. User microprograms loaded into a D-machine change its identity and destroy the Stack-machine previously loaded.

2. Input/Output Interface

Pivotal to the operation of the Burroughs system is the input/output interface. Only one processor, the IOP, communicates with peripherals, and the other D-machines, configured as Stack-machines, must compete for its services. The IOP communicates asynchronously, using a conventional 'handshake' method. Since all interpreters have access to the main memory module, a communications link has been established using the upper two 32-bit words of main memory. If a Stack-machine wishes to communicate with the IOP, it places a message into address 65,535 known as the 'mailbox',

and issues an interrupt (INT) to the IOP. The IOP periodically tests INT, and if set, will retrieve the contents of the mailbox (and mailbox + 1 if required) and perform the desired operation. The other Stack-machine is locked out from interrogating the IOP until it has completed processing the request. Normally, the operation requires transferring a buffer to some output device. When the IOP has completed honoring the request, it places a completion code in the mailbox and sets INT for the Stack-machine requesting the I/O. This interpreter must halt execution and check mailbox to see if the I/O was performed successfully, completing the handshaking process. This protocol permits both Stack-machines to perform input/output independently of each other, provided both maintain strict memory boundaries.

Another function of the IOP is interfacing character code formats between the peripherals and the other two D-machines. When the machines are configured as Stack-machines, characters are passed to the IOP in 6-bit BCL (Burroughs Common Language). The IOP must convert this character set to ASCII for output to the line printer and CRT. A similar translation must be made for input data converting from either EBCDIC or ASCII depending on whether the input source is the card reader or the CRT.

3. Memory Interface

Since all three D-machines must share the 64K of main memory, a priority scheme was developed to resolve

memory reference conflicts. The main memory module is actually a single-ported, 32-bit word, core memory which can be made to appear multiported using a switch interlock unit (SWI) developed by Burroughs. The switch interlock controls the main data bus of the system, and resolves conflicts using a priority scheme. The D-machine with the highest priority is the IOP, with the priority of the other two machines being relative to their physical proximity to the IOP. Once a memory reference has been made, a D-machine may continue execution without waiting for a completion signal from the switch interlock. Although this technique of memory referencing minimizes unnecessary delay, it restricts the program from changing the read or write addresses or the content of MIR (write only) prior to a completion signal.

C. MICROINSTRUCTION TIMING

The Burroughs D-machine initiates a microinstruction once every clock cycle. The D-machines utilized for the AN/UYK-20 emulation operated from a one MHz internal clock, which produced a clock pulse once every microsecond. A D-machine designed with an eight MHz clock, emitter-coupled logic (ECL), and a faster memory cycle time, however, could execute eight times faster. This implies that advances in circuit technology can permit emulations to achieve improved speed and performance with no change in the microprograms.

Every microinstruction is executed using one or more sequential time periods, called phase 1, phase 2, and phase

3. A phase is a constant interval of time equivalent to one clock duration measured from the trailing edge of each successive clock pulse. Some microinstructions only require phase 1 to complete execution. Some require phase 1 and phase 3, and still others require phases 1,2, and 3. A new microinstruction is initiated at each clock cycle, allowing for overlapping of microinstruction execution in phase 1 and phase 3.

Microinstructions consist of two types. In a type 1 microinstruction, events can take place in all three phases:

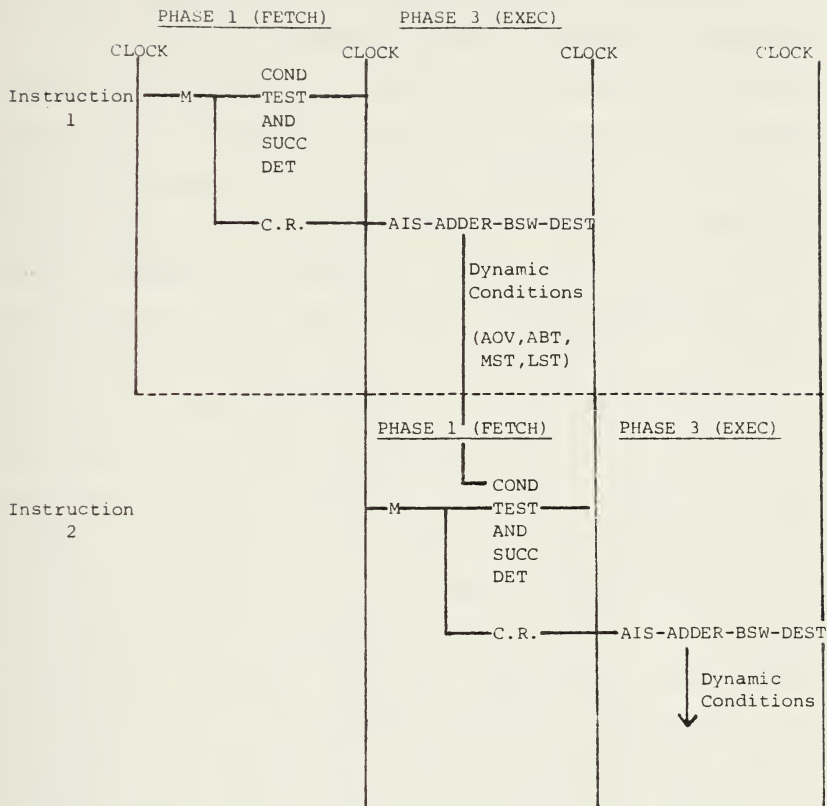
Phase 1: condition testing, (conditional) external operations or (conditional) logic operation initiation after completion of a prior logic operation, and successor M-memory address control.

Phase 2: a holding phase for phase 3 logic operation controls.

Phase 3: the completion phase for logic unit operations and destination register gating specified by logic operation.

During the optional phase 2 period, a type 1 microinstruction execution completion is held in abeyance while a subsequent type 2 instruction is executed. A type 2 microinstruction requires only phase 1 to complete execution, and involves literal assignments to three registers: LIT, SAR, and AMPCR. Phase 2 may also be initiated if the

next sequential type 1 instruction does not execute its conditional logic operation and therefore can complete its execution in phase 1 (Figure IV-3). Appendix D of Ref. 6 has a complete discussion of microinstruction timing.



M - MPM ACCESS TIME
 COND TEST AND SUCC DET - CONDITION TEST AND SUCCESSOR DETERMINATION
 BSW - BARREL SWITCH
 DEST - BARREL SWITCH OUTPUT DESTINATIONS; I.E., REGISTERS (B,CTR,ETC.)
 AND THEIR INPUT LOGIC
 C.R. - COMMAND REGISTER AND ASSOCIATED LOGIC
 AIS - ADDER INPUT SELECTION FROM COMMAND REGISTER

Timing Analysis, Type I Instructions

Figure IV-3 [17]

D. TRANSLANG

Microprogramming on the D-machine is accomplished using a microtranslator/assembler called TRANSLANG. TRANSLANG allows the programmer to write microinstructions mnemonically without concentrating on the bit patterns that compose the microinstructions themselves. TRANSLANG is written in ALGOL, the language of the B6700 Stack-machine. Nearly the entire language of TRANSLANG is composed of reserved words recognized by the ALGOL program. Each reserved word has a special meaning which causes the translator to construct particular microinstructions. A TRANSLANG instruction is equivalent to one microinstruction consisting of the set of parallel D-machine functions performed during the clock phases. TRANSLANG is a free form language and instructions may be written in almost any order. Multiple instructions may appear on a line, separated by a period '.'. TRANSLANG constructs include iterative mechanisms, input/output, assignment functions, control transfers, and Boolean, and computational operations. In addition, TRANSLANG permits label definitions and symbolic references for program control flow. Reference 6 is the programming manual for TRANSLANG and contains the complete syntax for the language. Appendix A of Ref. 10 documents additions to the TRANSLANG instruction repertoire.

A microprogrammer may construct complicated microinstructions that perform many different tasks, some interacting closely with D-machine clock timing. Microinstruction

gating to several devices permits a single TRANSLANG instruction to accomplish some or all of the following actions:

- a. test a condition.
- b. set/reset a condition.
- c. initiate an external operation.
- d. add.
- e. shift the result of an add.
- f. store the result into several registers.
- g. increment a counter.
- h. complement a shift amount.
- i. determine the successor microinstruction.

By judiciously composing his microprogram, a programmer may minimize execution time by taking advantage of microinstruction phase overlap and using highly parallel microcode.

The TRANSLANG assembler constructs an object program consisting of non-relocatable 56-bit microinstructions. TRANSLANG maintains a cross reference table that resolves label references during assembly. The object code created is stored on a disk and may be loaded into the micromemory of a D-machine using a special control word recognized by the operating system. Once loaded, the D-machine assumes the control structure dictated by the users microprogram.

V. AN/UYK-20 EMULATOR

A. EMULATION DESIGN

1. Functional Components

The architecture of the AN/UYK-20 emulator microprogram was developed using general guidelines provided by references and previous emulation experience on Burroughs D-machines [10]. The first decision incorporated in the emulator design was to integrate the entire emulation within one D-machine. Since the D-machines had the capacity to handle nearly 8K of microinstructions, no microprogramming capacity limitations were envisioned. The design objectives of a modularized, well-documented, structured microprogram could also be realized.

With the emulator entirely contained in one D-machine, several secondary benefits also existed. First, the emulator was more immune to hardware problems. If one D-machine was malfunctioning, the emulator could still be run on the alternate D-machine. Second, it was possible to have two AN/UYK-20 emulators resident in the system at one time. Not only would two emulators speed up testing of the individual emulation, but they would also permit their eventual use in a system configured for AN/UYK-20 multiprocessing. The third and final benefit of a totally integrated

emulator was recognized during the design of the input/output controller (IOC). Since the AN/UYK-20's IOC was capable of independent processing, an emulation of its IOC would not be possible within the same D-machine. An emulation of the IOC could be accomplished in a second D-machine, which would behave as an independent channel for the D-machine configured as the AN/UYK-20 processor. Although this emulation does not attempt to emulate the AN/UYK-20 IOC, the fact that a second D-machine exists makes its implementation a realistic extension to the project.

The emulator program organization was created following the basic guidelines of Ref. 17. The loader occupied the lowest section of M-memory with the emulator microcode following sequentially. Microprogram control passed from the loader to the emulator via the execution of a 'G' card which signified execution commencement.

The emulator microprogram was organized into three modules positioned such that forward address referencing would be minimized in the TRANSLANG assembler to save time and space. The utilities section was in the lowest portion of the emulator, since its routines were referenced frequently by the succeeding sections. Individual subroutines within the utility section were organized alphabetically.

The instruction and memory fetch routines comprised the next module. These routines incorporated all fetch options available in the AN/UYK-20 emulator.

The opcode routines occupied the last section of the emulator. The opcodes were arranged numerically with further indexing determined by the remaining fields of the individual instruction. Figure V-1 shows the M-memory mapping of the AN/UYK-20 emulator layout. Appendix F contains the emulation program listing.

2. Main Memory Organization

Of primary importance in the emulation design was the logical organization of the Burroughs system's main memory. Since the AN/UYK-20 was a 16-bit word machine, it was decided that only the lower half-word of a Burroughs 32-bit word would be used by the emulator. This design restriction permitted the addressing structure of the AN/UYK-20 to be directly projected on the D-machine. A one-to-one correspondence between the memory address of the AN/UYK-20 and the Burroughs system was also achieved.

Since the number of high-speed registers available in the D-machine was small, a 1K portion of main memory was reserved for the AN/UYK-20 addressable register set, the page address registers, the temporary storage space, and the emulation buffers. The mapping of the AN/UYK-20 high-speed registers to main memory greatly simplified the microprogramming requirements of the emulation, but added considerable execution time overhead. Memory access times for the mapped registers were much slower than the actual transfer

0000

LOADER
UTILITIES

INPUT/OUTPUT CONTROLLER
FETCH
OPCODE ANALYSIS
OPCODE 00
OPCODE 01
OPCODE 02
OPCODE 03
• •
• •
• •
OPCODE 74
OPCODE 75
OPCODE 76

AN/UYK-20 EMULATION ORGANIZATION

Figure V-1

rates of the AN/UYK-20 registers. Figure V-2 shows the complete main memory mapping of the emulation reserved storage area.

3. Emulation Program Status Word

Although the emulation duplicated all the AN/UYK-20 registers, the registers which comprised the program status word (PSW) possessed unique characteristics. Status register 1 was combined with the program address register to form a single 32-bit PSW. The emulator's PSW always co-existed in the A1 register of the D-machine and in main memory during execution of AN/UYK-20 programs. The fields of SR1 were modified to include certain emulator toggles, along with the normal condition bits (Figure V-3). The condition bits for DMA and non-destructive read only (NDRO) mode were removed from the SR1 since they were hardware features of the AN/UYK-20 that would not be emulated.

Status register 2, the remaining 16 bits of the AN-UYK-20's PSW, was not resident in any D-machine registers during emulation execution for two reasons: the emulation could not afford the luxury of 48 bits of reserved register space, and SR2 was less frequently referenced than SR1 and the P-register. Consequently, SR2 had to be read from its reserved location in main memory. The contents of the upper 16 bits of SR2's memory location also contained additional emulation toggles which were used by the debugger package (Figure V-3).

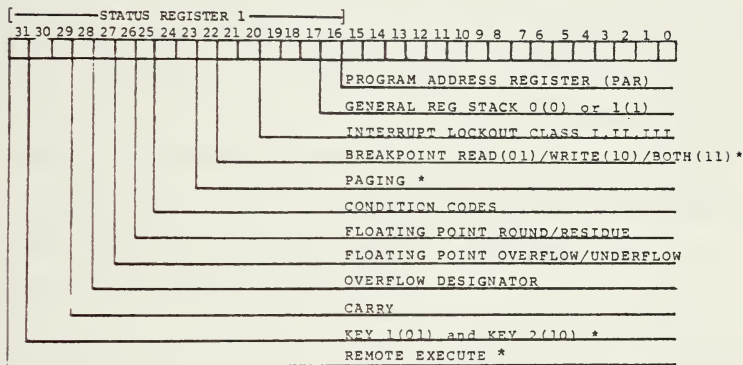
MAIN MEMORY MAPPINGS

DECIMAL ADDRESS	OCTAL ADDRESS	USE

0 - 15	0 - 17	GENERAL REGISTER STACK 1
16 - 31	20 - 37	GENERAL REGISTER STACK 2
32	40	PROGRAM STATUS WORD
33	41	BREAKPOINT REGISTER
34	42	STATUS REGISTER 2 (SR2)
35	43	NEXT LOAD ADDRESS
36	44	CLOCKTIME
37	45	REAL TIME CLOCK
38 - 43	46 - 53	WORKSPACE (TEMP STORAGE)
44 - 49	54 - 61	STACK (TEMP STORAGE STACK)
50 - 53	62 - 65	I/O COMMAND WORDS (IOCW)
54 - 119	66 - 167	UNUSED
120 - 121	170 - 171	HEX ADDRESS FOR INPUT
122 - 141	172 - 215	INPUT CARD BUFFER
142 - 152	216 - 230	UNUSED
153 - 185	231 - 271	OUTPUT PRINT BUFFER
186 - 205	272 - 315	CRT BUFFER
206 - 229	316 - 345	ERRORLIST
230 - 767	346 - 1377	UNUSED
768 - 1023	1400 - 1777	PAGE ADDRESS REGISTERS

Figure V-2

ACTIVE PSW: RESIDES IN LU REGISTER A1 (MEMORY ADDRESS 32)



[— STATUS REGISTER 2 —]

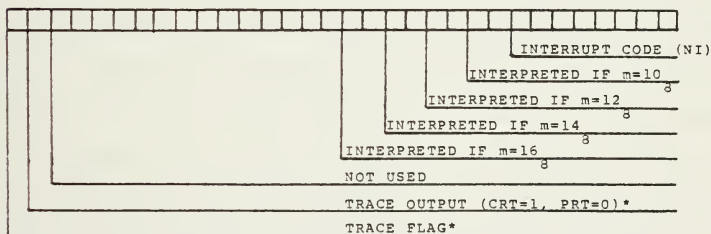


Figure V-3

4. D-Machine Registers

with only a limited number of high-speed registers available in the D-machine, the emulation design had to include a well-developed plan for their usage. Since only seven registers in the D-machine were 16 bits or longer, they were used exclusively for manipulating the AN/UYK-20 addresses, instructions, and data. The register environment had to be consistent throughout every execution cycle to allow utility routines to be called in the same manner by all opcode subroutines. The primary goal of the emulation was to use as few memory references as possible to conserve execution time and memory space. Judicious use of the existing registers was a necessity.

Several factors had to be considered before selecting a register for a particular function. The most important consideration was its flexibility within the D-machine. The B register, for example, was used as a general purpose register, since its contents could be gated through a masking filter prior to being utilized. A second factor was the type of operand it could contain. Double-word operands (32-bit) could only be stored in the 32-bit logic unit registers while 16-bit operands could also be stored in the memory control unit registers.

The A1 register contained the emulation's 32-bit program status word (PSW) at the commencement of the emulator program. It was not affected by individual instruction

microcode, except when incrementing the PAR, or when a particular instruction modified the PSW. Emulator toggles resident in SR1 could not be altered by an AN/UYK-20 instruction because their settings were independent of program execution.

The A3 register held the instruction word for the duration of its execution cycle. Each field of the instruction could be decoded and interpreted from the A3 register without having to retrieve it from memory. Once the instruction had been completely decoded, A3 was made available as a scratch pad register.

The A2 and B registers were used as scratch pad registers during each opcode execution cycle. In general, their contents were volatile, except when they were specifically documented in the the program listing. The contents of A2, for example, was not altered in the EMULIN subroutine, because of its use in the calling fetch routine. A2 and B were manipulated as either single or double-word operands during the arithmetic operations.

The only remaining logic unit register was the memory information register (MIR). MIR was used for storing information into memory and as a temporary storage location. Intermediate results were deposited in MIR during instruction execution and returned through the B register.

The base registers, BR1 and BR2, were used as storage for addresses and single-length operands, and for

temporary storage of intermediate results. In addition, all memory addressing in the emulation was accomplished using the lower 8 bits of BR2 and MAR (MAR2). These memory control unit registers had to be used carefully, because they required a sequence of several microinstructions to properly reference their contents.

B. LOADER

The loader incorporated into the AN/UYK-20 emulation provided a simple mechanism for loading AN/UYK-20 instructions into main memory (S-memory) of the Burroughs microprogramming system (Figure V-4). Its control word repertoire was flexible, allowing a variety of AN/UYK-20 program environments. Job control statements were included to execute and halt individual programs anywhere in S-memory.

The loader module consisted essentially of a scanner and a translator written in the microcode. Information was read into a 20-word buffer from cards or CRT input, then the buffer contents were scanned for control code consisting of one or more characters. Once these characters were interpreted, control was passed to the translator section which decoded the rest of the data in the buffer and performed the required function. The translator section consisted of a variety of routines that handled specific control words in the loader repertoire. The loader control statements, however, had to appear in a logical sequence (See Appendix A). All loader control statements are contained in Appendix B.

AN/UYK-20 LOADER

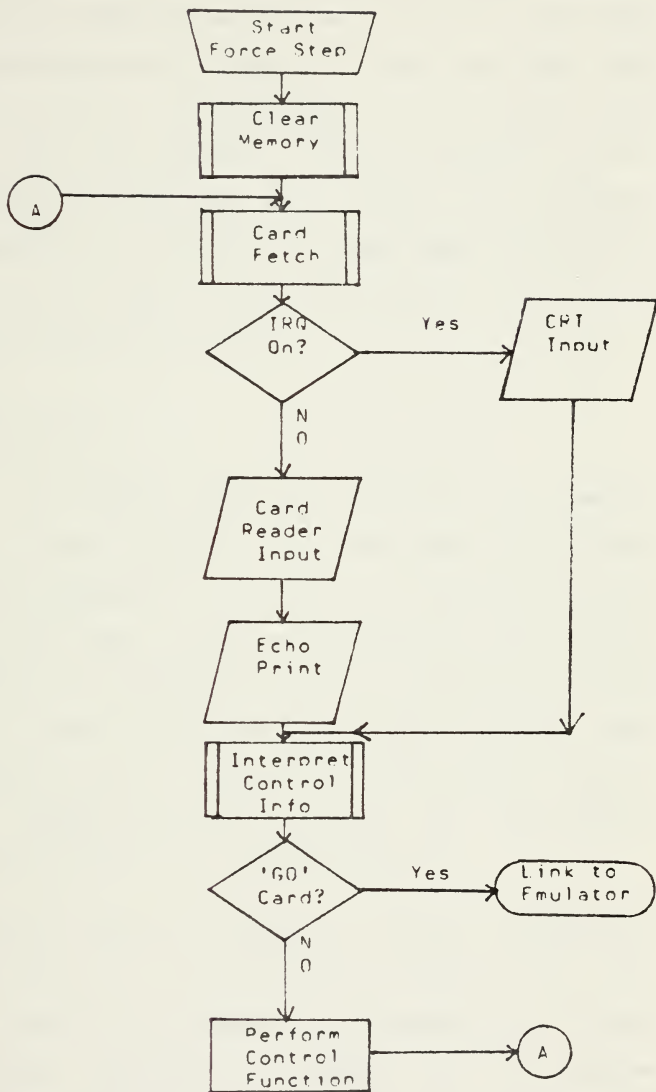


Figure V-4

The actual interface pipeline between the loader and the emulator consisted of two small emulator utility routines which started and stopped the external clock of the Burroughs microprogramming system. These routines were inserted for emulation timing purposes, and provided a 'stop watch' for AN/UYK-20 programs. The time recorded (in milliseconds) by this 'stop watch' was placed in a reserved memory location in the emulation memory map, and could be read using either a trace control instruction ('T'), or a machine status control word ('M').

C. THE FETCH MODULE

In order to emulate AN/UYK-20 execution and memory referencing, fetch microcode was developed which incorporated memory addressing algorithms and instruction fetch routines. Since both data and instructions were equally accessible from the processor, the memory addressing scheme was closely linked to the instruction fetch concept. Data and instructions could be interspersed throughout memory, and proper program execution required that the program address register point to an instruction word.

The emulation used two routines for memory addressing, EMULIN for reading, and EMULOUT for writing (Figures V-5, V-6). These subroutines performed both paging and break-point checking, depending on toggles set in the program status word. Paging was incorporated into the emulation in order to gauge the execution overhead required in emulating

the AN/UYK-20's paging scheme. The paging scheme implemented in the emulator divided main memory into 256-word pages, instead of 1024-word pages used by the AN/UYK-20. Since the Burroughs D-machine was organized for 256-word pages, the microprogramming required for the paging was straightforward. The 256 page address registers resided in the emulator's memory mapping, each initialized to the page number corresponding to their relative address (0-255). The paging algorithm imitated the AN/UYK-20's method of page addressing, and included the setting of a page modification bit.

The breakpoint option was added to provide a method of debugging AN/UYK-20 programs, once the emulation was completed. EMULIN and EMULOUT tested toggles set in the PSW to determine if breakpoint read, write, or both was desired.

The memory addressing convention required all memory references from 1K to 64K to use EMULIN and EMULOUT. All memory references to the memory mapping area (0-1023) did not use these routines, but instead utilized absolute memory referencing microcode.

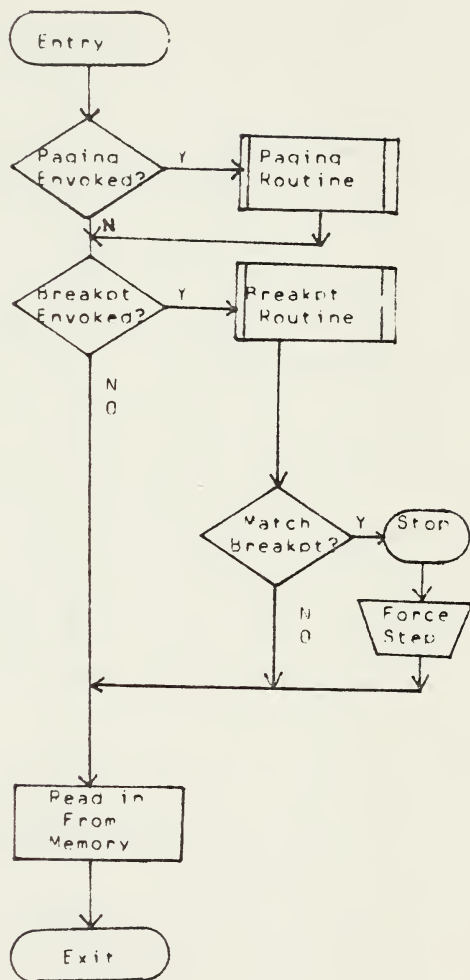


Figure V-5

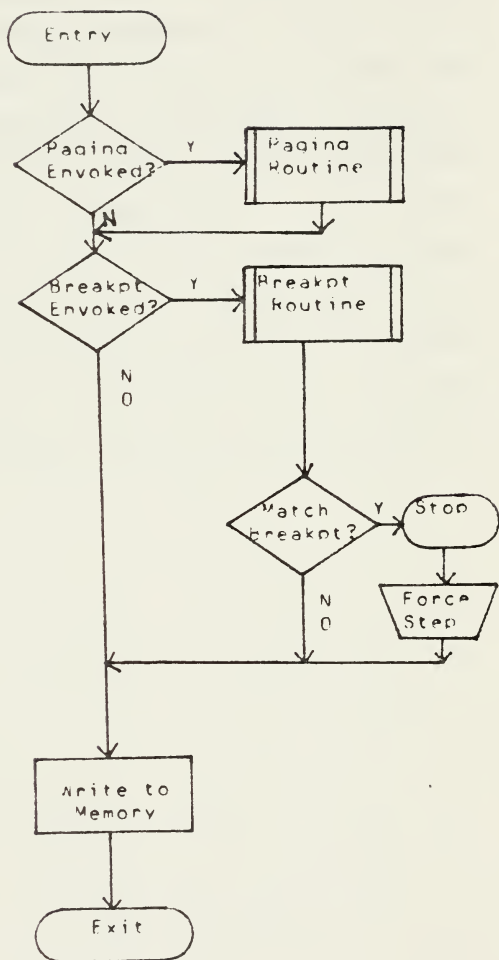


Figure V-6

The instruction fetch routine (IFETCH) retrieved instructions from main memory based on the contents of the program address register. Since IFETCH used EMULIN to read the instructions from memory, it could operate in a paging environment, with or without breakpoints (Figure V-7). IFETCH was also responsible for incrementing the PAR, and for testing the trace toggle prior to fetching an instruction. IFETCH was capable of retrieving any instruction word in the program address space (1024-65,535). In the event that the upper memory limit was reached, IFETCH would set the PAR to 1024 and continue execution. Trace toggle testing was inserted into IFETCH as part of the built-in debugging package. Since IFETCH was called prior to every instruction, it was the logical choice for placing a call to the debugger.

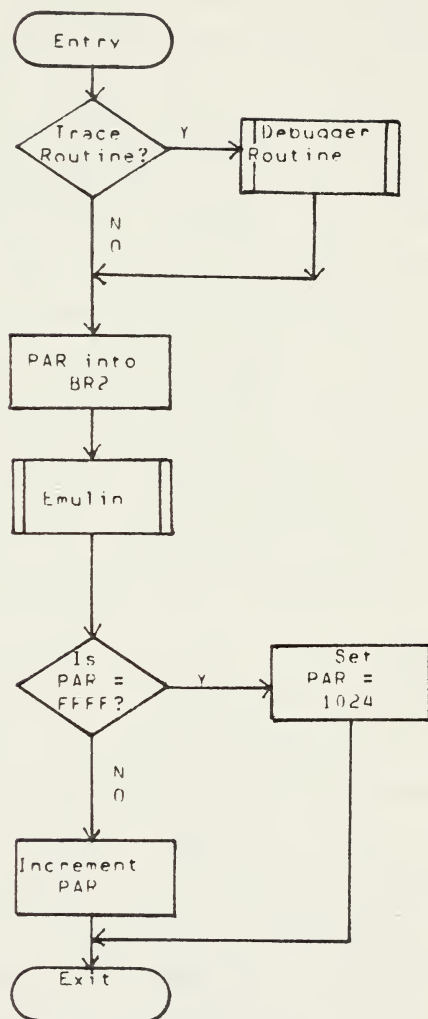


Figure V-7

D. OPCODE IMPLEMENTATION

All of the 205 individual instructions emulated were microprogrammed using an identical instruction decoding mechanism. The routines that performed the required operations were terminal nodes on a large tree network, whose root was the OPCODE routine. OPCODE fetched an instruction and isolated the operation code field. The binary value of the opcode field was an index to an operation jump table containing individual opcode M-memory addresses. Within each opcode routine was microcode which isolated the sub-function 'f' field of the instruction and used its value as an index to the next level of opcode analysis. Depending on the opcode, this last jump could identify which instruction was to be performed. If it did not, further analysis of the 'm' or 'a' fields provided the final index to the instruction. Instruction formats are described in Appendix C.

After the instruction had been executed, control passed back to the opcode routine, and then the execution cycle was repeated for the emulation of the next AN/UYK-20 instruction. The AN/UYK-20 programmer could cause this microprogram loop to be exited by either inserting an executive return instruction (03,0,a,00) which caused a 'priority interrupt' and halted program execution, or by coding an instruction that was not implemented, not assigned, or caused a division overflow. The last three cases caused an execution fault, while the former resulted in normal program termination (Figure V-8).

AN/DYK-20 EMULATION GENERAL STRUCTURE

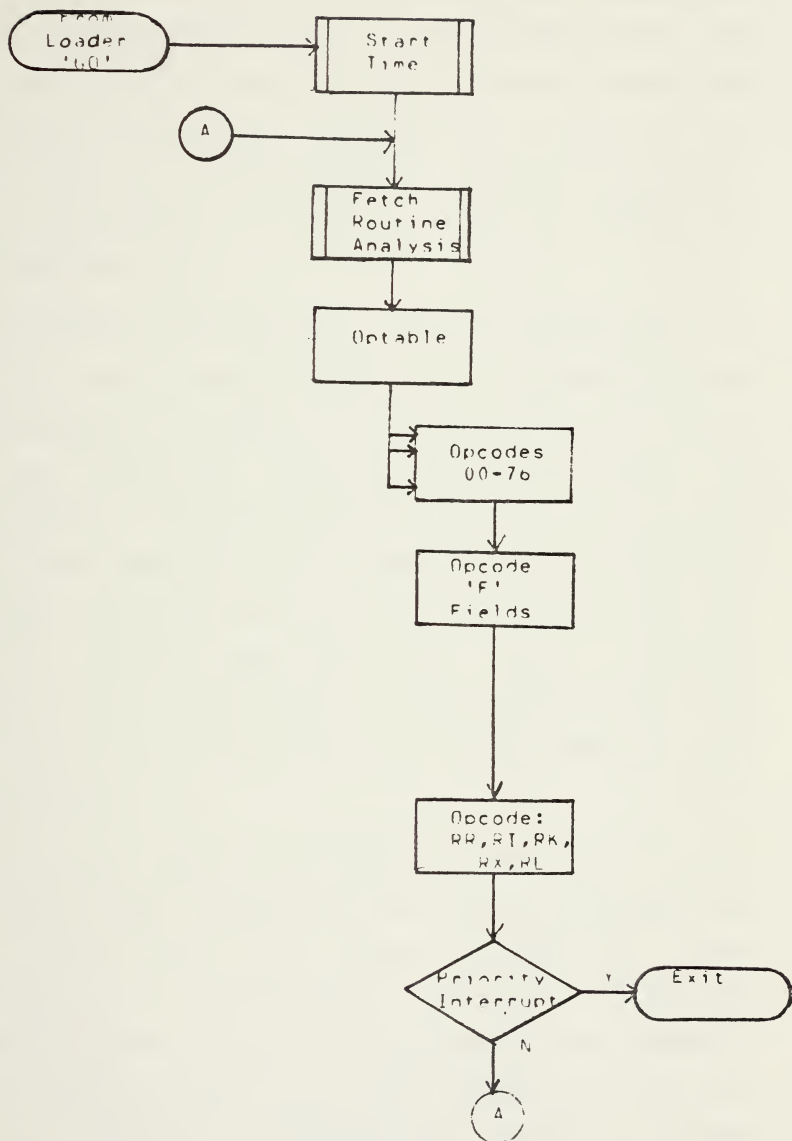


Figure V-8

The instruction fetch mode of OPCODE assumed that the PAR always pointed to an instruction word. Double-word instructions always had their 'y' field fetched after they were determined to be two words in length. Conditional double-word instructions performed their condition test before the 'y' field was fetched. If the test failed, the PAR was incremented by two prior to returning to OPCODE for continued execution.

The OPCODE routine was also written to accommodate the AN/UYK-20 'remote execute' instruction. When this operation was performed, a bit was set in the PSW which would indicate that one instruction out-of-line was being executed. For this operation, the current PSW was stored in memory, and the PAR was loaded with the address of the instruction to be executed. The OPCODE routine always checked the remote execute bit during an instruction cycle. If the bit was set, it would fetch the instruction indicated by the remote execute PAR, and restore the actual PAR, incremented by two, into the PSW.

Some of the opcode repertoire of the AN/UYK-20 was not emulated. Those instructions that were not emulated, however, retained slots in the opcode hierarchy for future inclusion. Any instruction not implemented by the emulator caused the machine to fault, and printed an error diagnostic on the selected output device ('NOT IMPLEMENTED - EXECUTION ENDS '). Similarly, locations were reserved for those instructions not assigned by the AN/UYK-20 were reserved

locations in the emulation . This permitted the emulator to be responsive to any future AN/UYK-20 hardware modifications. Whenever an instruction to be executed was not assigned, the emulator generated a fault interrupt and printed an error diagnostic on the selected output device ('FAULT INTERRUPT - EXECUTION ENDS').

E. UTILITIES

Although each emulated instruction performed different operations, each depended upon a common set of utility subroutines to accomplish their task. These subroutines varied in complexity, but each performed a function that contributed to successful instruction execution. A simple operation often required register addressing, condition code setting, and memory addressing, before the task was completed.

Utility subroutines were included in the emulation whenever feasible to simplify microprogramming and to alleviate programming redundancy. These subroutines were called using the successor command constructs available in TRANSLANG. Depending on the purpose of the utility routine, parameters were passed via D-machine register(s) or condition bit(s). This information was utilized by the utility in determining what operation was to be performed. In the carry subroutine, for example, a local condition bit was passed which indicated the appropriate condition code to be inserted into the PSW. A more complex example, the RX

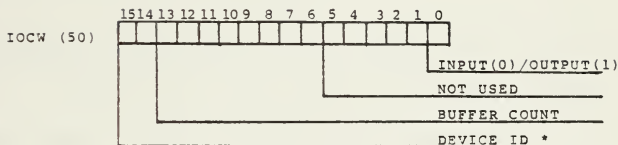
format utility routine, required two parameters to be set by the instruction. Register A3 contained the instruction word and LC2 was set or cleared depending on whether or not byte formatting was required. The RX routine called other routines and could perform considerable processing before the final result, the effective operand address, was returned to the calling routine via the B register.

The utility section encompassed a number of routines which performed complex data manipulation. Arithmetic utilities for multiplication, division, and square root were accessed by nine separate AN/UYK-20 instructions. Indirection routines, which were called by the RX format routines, emulated the AN/UYK-20 cascaded addressing capabilities. A general purpose move subroutine permitted up to 256 cells of main memory to be moved from one location to another. This routine was used by the emulator's error diagnostic utilities, as well as the load and store multiple address register instructions.

F. INPUT/OUTPUT CONTROLLER

Although the AN/UYK-20's IOC was not emulated, several of its design features were imitated in creating a general purpose input/output controller for the emulator. The input/output command instruction (35 RR) initiated the I/O sequence, and reserved several cells in the memory mapping for I/O control words (Figure V-9). These control words contained fields which indicated what peripheral device was

AN/UYK-20 EMULATION
INPUT/OUTPUT COMMAND WORDS



BUFFER ADDRESS
THE MICROCODE ALTERS THE IOCW + 1
DURING BUFFER TRANSFER



BUFFER SIZE
USED FOR CRT OUTPUT



NUMBER OF SECTIONS
USED FOR DISK TRANSFERS (NOT IMPLEMENTED)
* CODE: 00 - CRT
01 - PRT (OUTPUT)/CRD RDR (INPUT)
10 - DISK (NOT IMPLEMENTED)

Figure V-9

selected, the number of buffers that would be passed, whether input or output was desired, and where the buffer was located. Two additional words were reserved for control data required to interface with the disk and the CRT. The disk input/output microcode was not incorporated into the controller, but the framework was provided so the IOC could be readily inserted in the future.

The emulator's IOC section was located in the utility section of the emulation, and operated asynchronously with the Burroughs IOP. Since the IOC was collocated with the emulator in the same D-machine, it was not capable of independent processing. Once it was initiated, emulation execution waited until input/output was completed. The emulation had to use the Burroughs Common Language, since the IOP was microprogrammed to accept only this character set from other D-machines.

In order to transfer a 33-word line printer buffer to the IOP, the AN/UYK-20 emulator IOC had to use 66 AN/UYK-20 words. In order to send 20 words to the CRT, the IOC had to construct a 40-word buffer. The COMPRES subroutine packed an AN/UYK-20 buffer of 66, 16-bit words into a 32-bit, 33-word buffer, suitable for output to the IOP.

Similarly, on input, a 20-word IOP buffer from the card reader or CRT expanded into a 40-word AN/UYK-20 buffer. In this case, the EXPAND subroutine split every packed 32-bit word of the IOP's buffer into two 16-bit words, suitable for processing by the emulator. These additional data transformations were required because of the buffering requirements of the Burroughs IOP.

VI. EMULATION TESTING

A. METHOD OF TESTING

The fundamental testing technique utilized throughout the development of the emulation consisted of three distinct phases: 1) each module was independently assembled and debugged until successful assembly was achieved, 2) each program segment was then tested for accuracy of the intended operation, and 3) the composite emulation program was tested under actual program conditions allowing for interaction among several modules. A debugging package, which was developed early in the emulation project, was the primary test vehicle for verifying emulation coding. Development and testing of the loader was, however, completed prior to the creation of the debugger.

Loader testing was accomplished by monitoring the control panel lights and synthetically halting program execution via the insertion of 'WAIT' statements, forcing the desired register to be transferred to 'MIR', and then re-examining the panel lights. This process was extremely tedious and time consuming but proved to be an invaluable tool for recognizing peculiar TRANSLANG constructs and microinstruction execution side effects.

Each module was subjected to an extensive desk checking process in order to reduce trivial assembly errors before running it on the machine. After a successful assembly had been achieved, the code was merged with previously existing assembled modules. The emulator was expanded as more modules were added, with utility routines being incorporated prior to the opcode programs.

Initially, the loader was designed, programmed, and thoroughly tested prior to the microprogramming of any AN/UYK-20 instructions or utilities. With the loader implemented, the emulation of the UYK-20 instruction repertoire could proceed with a minimum of loader induced problems.

Independent opcodes and various utility routines were added to the previously assembled programs. The final emulation consisted of a total of 205 opcodes, a set of utility programs, and a workable loader.

In the next phase of testing, every module was subjected to a representative number of test cases which demonstrated how closely they compared to the documented AN/UYK-20 operation. Artificial environments were created to subject every opcode to a variety of situations. Whenever the operation of the opcode disagreed with the documented AN/UYK-20 operation, the opcode's function was thoroughly researched. The opcode's side effects were categorized and questions formulated. Often the answers could only be obtained from the Univac field engineer.

To illustrate the complexity of testing, an add instruction was tested with numerous operand combinations: two positive operands, two negative operands, one of each sign yielding a negative result, opposite signs producing a positive result, and opposite signs producing a zero sum. During each addition operation, the overflow, carry, and condition bits had to be monitored in status register 1 to verify their appropriate setting. This level of detail was achieved with all of the implemented opcodes in order to produce an efficient and accurate emulation.

Throughout the entire testing scenario, which composed 20% of the emulation project, the debugger routine (DUMPREG) provided the necessary information for examining opcode execution. A representative sample debugger output is provided in Appendix D.

DUMPREG permitted a snapshot of both AN/UYK-20 general register stacks, PSW, SR1, and SR2, in addition to the D-machine registers (A1, A2, A3, BR1, AMPCR, MIR) and the Burroughs external clock. DUMPREG possessed sufficient flexibility to be incorporated into the microcode at any point. In the final emulator, however, the debugger is user specified, and will dump the AN/UYK-20 emulator environment either at every instruction fetch and program stop, or when called by a loader control card.

B. SAMPLE TEST PROGRAMS

After subjecting the entire emulation to extensive testing, some representative test programs were developed to demonstrate the feasibility of the emulation and its capabilities and performance as compared to an actual AN/UYK-20. There were two programs which were selected because they incorporated numerous emulation features. The two programs were the solution of simultaneous linear equations by Cramer's rule and generation of prime numbers. It must be noted that streamlined program design was not emphasized but rather utilization of a variety of opcodes and features of the emulation.

The program for solving linear equations contained a total of 28 opcodes, requiring 28 opcode execution cycles and 43 instruction fetches. The program demonstrated all four fundamental mathematical operations, numerous store and load functions, a comparison test and a jump instruction. The capability of performing card reader input and output was added when the emulator IOC was completed.

The prime number program demonstrated 30 instructions which required 116 opcode execution cycles, and 122 instruction fetches. This program illustrated numerous comparison tests, looping structures, several jump instructions, a load multiple instruction, addition, and division. The test programs are included in Appendix E.

C. TEST RESULTS

The performance analysis of the test programs consisted primarily of running numerous test cases, examining the results for accuracy and computing the total time required to execute the emulated AN/UYK-20 programs. The timing of the programs was accomplished by using an external clock available on the ICP. The clock time provided a fairly close representation of the emulation execution time, but it cannot be considered a completely accurate measure since the emulation must interrogate the IOP to retrieve the external clock contents. Approximately 50 microseconds are used when sampling the clock.

The time requirements of the AN/UYK-20 program execution were hand-calculated by summing the published instruction execution times as presented in Ref. 21. The emulation performance ratio (EPR) was computed merely to give an approximate indication of the emulation performance. The EPR is the ratio of measured Burroughs emulation time to the calculated AN/UYK-20 execution time. Two EPR figures are recorded: one with paging implemented and one without. The paging EPR figure is significant only in that it indicates how much additional overhead must be incurred when emulating the paging mechanism of the AN/UYK-20. The required additional execution time was about 26%. Naturally, paging overhead is directly proportional to the number of instruction fetches or memory references performed during a program.

The results of program testing are as follows:

	CRAMER'S RULE	PRIME NUMBERS

Number of Opcodes	28	30
Number of Fetches	43	122
Execution Cycles	28	116
Time w/o paging	5000 usec	13000 usec
Time with Paging	8000 usec	17000 usec
AN/UYK-20 Time	78 usec	193 usec
EPR w/o Paging	64 :: 1	67 :: 1
EPR with Paging	103 :: 1	88 :: 1

These figures represent only approximate comparisons of the two machines. These computations provide an estimate of emulation characteristics. An effective EPR without paging was projected to be 65::1.

VII. SUMMARY AND RECOMMENDATIONS

A. EXPERIENCE WITH HARDWARE

The emulation project provided the unique opportunity of learning about two computer systems. The Burroughs D-machine demanded a detailed knowledge of hardware operation, as well as a thorough understanding of the microprogramming language, TRANSLANG. The computer architecture and processor capabilities of the AN/UYK-20 had to be investigated and then integrated into the control store memory of the Burrough's D-machine.

On several occasions, hardware malfunctions with the Burroughs equipment prevented normal system operation. The card reader was inoperable for several weeks, and the disk drive unit had to be repaired several times. During the final three weeks of project development, one D-machine ceased to function properly. This restricted emulation testing to the remaining D-machine.

Although these hardware difficulties impeded normal progress of the project, they did not prevent the emulation from successfully being completed. If a hardware problem prevented emulation testing or debugging, other modules were designed and testing was postponed. This permitted continual emulation development regardless of the hardware

status. In addition, considerable time and effort was invested in trouble-shooting hardware malfunctions, so they could be isolated, diagnosed, and repaired.

B. LESSONS LEARNED

The emulation project brought together many different computer science techniques and disciplines which will be useful in future computer science endeavors. A great deal of experience in both computer architecture and operation was gained in two different types of computers. Microprogramming provided new insight into computer design and revealed many potential applications for programmable control store machines.

Since emulations normally require a large development effort, this project had to incorporate judicious system design and project management principles in order for it to be completed successfully. Careful monitoring of critical stages of the emulation, and coordination of the programming effort to meet scheduled requirements, was necessary throughout this research. The small programming team concept proved to work extremely well in this project.

Finally, several software practices were strictly followed that proved to be invaluable in constructing the emulation. First, modular programming succeeded in partitioning the emulation into discrete modules which could be designed, coded, tested, and implemented individually. The

emulation was constructed in segments, using the previously verified modules as a test bed for the new modules being built. Structured programming and prolific documentation were useful in developing each microprogram routine because they permitted each team member to understand the function of the program and how it could be used.

C. EMULATION PROBLEMS

The most significant problem of the emulation was not having had any experience with an AN/UYK-20 and not having anyone readily available with prior AN/UYK-20 experience. This lack of knowledge created some anxiety when attempting to analyze the ramifications of individual opcodes.

The idiosyncrasies of certain opcodes were not made self-evident by the AN/UYK-20 software manuals. Consequently, numerous code modules were redesigned when more detailed information was provided by a UNIVAC field engineer. This proved to be very time consuming, inefficient, and frustrating.

Another emulation difficulty was the lack of working registers in the host machine as compared with the target machine. While the AN/UYK-20 has either 16 or 32 general registers, depending on whether the second stack option is incorporated, the D-machine has effectively only seven workable registers containing 16 bits or more. Therefore, all AN/UYK-20 registers had to be mapped into S-memory which

created much longer register read/write times. This created significant register manipulation problems which in some cases required main memory references for instructions intended to be strictly register-to-register operations. Consequently, increased execution times resulted in a higher emulation performance ratio (EPR), decreasing the overall emulation performance.

D. RESULTS

Emulating the AN/UYK-20 on a Burroughs D-machine required a considerable amount of preparation and planning before any results were realized. An in depth analysis of each computer's architecture and operating characteristics was conducted to insure that an emulation was feasible in the allotted time period. From the inception of the project, the goal of the emulation was to implement a standard AN/UYK-20 processor. This decision was based on the capability of the D-machine and an estimate of how much time would be involved in developing, debugging, and testing the final product. Although this goal was achieved, it was felt more time could have been devoted to testing and verifying emulation operation.

The AN/UYK-20 emulation was a highly complex microprogramming project involving numerous data structures and transfer protocols. A total of 205 AN/UYK-20 instructions were emulated out of nearly 290 instructions in the repertoire (including all IOC, math pac, and clock interrupt

opcodes). AN/UYK-20 diagnostic programs and user programs will establish the validity of the emulator's construction.

E. RECOMMENDATIONS AND FOLLOW-ON TOPICS

Although 205 opcodes have been implemented, tested, and developed into a working emulation, there are still many challenging avenues to pursue in creating the complete emulation package. First, testing is a continuous process and should be performed in conjunction with code optimization. A comprehensive code optimization effort could improve the EPR without sacrificing code readability.

Second, the floating point and 'math pac' options could be implemented. The addition of floating point arithmetic, trigonometric, and hyperbolic functions would significantly strengthen the scientific capabilities of the emulation. This would be an extremely strenuous undertaking but would permit more tactical data applications of the emulation, increasing its value to the Navy.

One area which could be examined is to perform a comprehensive timing analysis between an AN/UYK-20 and the emulation. This could consist of collecting numerous benchmark programs from Navy AN/UYK-20 installations, where performance data could be accurately obtained. These programs could then be run on the emulator, and analyzed with the benchmark results. The feasibility of replacing or substituting emulation host machines for target machines could be

addressed and supported by the timing analysis study.

An emulation of the AN/UYK-20 input/output controller could be incorporated into the emulation without serious difficulty. Since a second D-machine is available, the IOC channel processor instructions could be emulated and inserted into that D-machine's control memory. The independent processing characteristic of the AN/UYK-20 IOC would be fulfilled using this arrangement.

Finally, when the Burroughs system is linked with the computer science department's PDP 11/50, the AN/UYK-20 emulator could be connected to that system's peripheral resources. This would allow future incorporation of an AN/UYK-20 ULTRA assembler and a CMS-2M compiler into the PDP 11/50 system which could then produce machine language object code files for the AN/UYK-20 emulator to execute.

APPENDIX A. AN/UYK-20 EMULATOR USER'S MANUAL

This description is designed to provide sufficient information to operate the AN/UYK-20 emulation program. It is assumed that the informal Burroughs D-machine manual in the Burroughs laboratory will supply adequate power-on instructions and solve any hardware operating difficulties which may arise.

The procedure for utilizing the AN/UYK-20 emulator can be divided into four phases:

- 1) selection of the necessary loader control cards (JCL).
- 2) selection of the AN/UYK-20 program instruction set.
- 3) implementation of phases one and two into the required card or CRT format.
- 4) actual hardware implementation on the Burroughs D-machine resulting in program execution.

Phase one can be achieved by selecting the desired loader control cards described in Appendix B. The card format is identical to the CRT format, except that the CRT requires the user to <carriage return> at the end of every line of input data.

Phase two is accomplished by creating the AN/UYK-20 program from a subset of the 205 emulated instructions.

Phase three consists of keypunching the desired JCL and AN/UYK-20 program in the format illustrated in Appendix C.

The resulting job deck will typically be assembled as follows:

?SMLoad TED/UYK20-OBJECT % loads the emulator into
micromemory

L 00004 % load the program into
page 4

C 00206 FAULT INTERRUPT-EXECUTION ENDS "

C 00214 NOT IMPLEMENTED-EXECUTION ENDS "

C 00222 DIVIDE OVERFLOW - FAULT ENTERED"

other desired JCL

AN/UYK-20 Program

03,0,a,00 % priority interrupt
(a = 00-17 octal) (mandatory card)

G % commence program
execution

M (or M1) % machine status (reg. dump
at termination)

E % end job card

Finally, phase four consists of the entire program deck being loaded into the card reader. It is assumed that the IOP is at address 0015 hex, the selected interpreter is at address 0549 hex, the line printer is 'READY', and the IRQ switch is 'off'.

The IRQ switch is a three-way toggle switch mounted on the right side of the interpreter. In the up position, IRQ is 'on', horizontally it is 'off', and the downward position is used for external functions.

If either the interpreter or the IOP is not at the proper starting address, clear them by depressing the 'CLEAR' button on each unit. If this procedure does not remedy the situation, consult the user's manual in the laboratory.

Upon reading the ?SMLOAD card, the system will load the AN/UYK-20 emulator object program into the micromemory of the selected interpreter. The program address counter (on the interpreter) will be at the beginning of the emulation program, address 0000 hex. At this point, the user can select CRT input and output by placing the IRQ switch to the 'on' (upward) position. If CRT input is not desired, leave the IRQ switch in the 'off' (horizontal) position. Next, force step the interpreter by momentarily depressing the FST button (uppermost push button on side panel of the interpreter). Do not hold in the FST button. This may cause some undesirable side effects.

After depressing the FST button, the AN/UYK-20 program is loaded into S-memory. If the input is expected from the CRT, the user must enter his program from the console. Otherwise, the emulator will request cards from the card reader. Once the program has been loaded and the 'G' card read, program execution begins.

After successful program termination, the program returns to the loader and asks for more input. At this point, the user may terminate his job, or start another load sequence. It should be remembered that the AN/UYK-20 emulator has been designed for monoprogramming execution. It executes one program at a time, but can execute any number of programs in sequential order if desired. When the job is terminated, the D-machine returns to its starting address (0000 hex) and awaits further processing. When the user returns to the start address, the system is effectively 'master cleared' since S-memory will be cleared prior to executing any further jobs. It is not necessary, however, to use the ?SMLOAD card for additional programs or program re-runs because the emulator object code still resides in micromemory.

If the results of program execution are not as anticipated, use of either a 'T' or 'T1' option (trace card) is recommended to provide the user with a fetch-by-fetch program trace with the output to the printer or CRT respectively.

APPENDIX B. LOADER CONTROL CARD FORMATS

CARD COLUMNS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	-	20

B	R																
	W																
	B																

C																	
D																	

E																	

G																	

I	1																
	2																

L																	

M																	
	1																

P																	

R																	

S	1																
	2																

T																	
	1																

Note: All numeric fields are in decimal.

LOADER CONTROL CARD DESCRIPTION

Control Card Identifier		Description
B	---	The 'B' card is used to implement the breakpoint feature of the emulation. This feature allows the user to specify a decimal address in columns 4-8. Column 2 must contain a R or W to breakpoint on a read or write operation respectively. The default condition is breakpoint on both read and write.
C	---	The 'C' card is used to insert character strings into memory. The character string starts in column 9 and continues until terminated by a quote symbol (") or the string reaches column 80. The decimal address where the character string will be written is given in columns 4-8. A blank or zero address field causes the character string to be inserted at the current load address.
D	---	The 'D' card is used to store decimal data from columns 16-20 into the memory address found in columns 4-8. A blank or zero address field causes the data to be inserted at the current load address.
E	---	The 'E' card is used to indicate the end-of-job and therefore is a mandatory control card for job separation.
G	---	The 'G' card or 'G0' card is used to start execution. The starting decimal address is in columns 4-8. The default value of a blank or zero address field will cause program execution to start address 01024.

- I --- The 'I' card or set index register card is used to store decimal data from columns 16-20 into the register designated in columns 7-8, into the general register stack (1 or 2) specified in column 2.
- L --- The 'L' or load card is used to partition memory into 256, 256-word (32-bit) pages and to load the program into the decimal page as referenced by columns 4-8. Pages 0-3 should not be used because they contain the required emulation register mapping and established workspace. The 'L' is a required control card, and it is recommended that it be the first JCL card.
- M --- The 'M' card or machine status card provides a register dump, wherever it is inserted. It is normally placed between the 'G' and 'E' cards in the JCL deck. If a 1 is placed in column 2, the machine status dump will be sent to the CRT. This dump will contain the current value of all AN/UYK-20 general registers, the PSW, SR2, next instruction address, the breakpoint address, and clocktime.
- P --- The 'P' card is used to implement paging.
- R --- The 'R' or reserve space card is used to reserve memory space as specified decimally in columns 4-8.
- S --- The 'S' card is used to simulate setting of the program stop switches (1 and 2) on the AN/UYK-20 maintenance panel. Column 2 must contain a 1 or a 2. Two cards are required if both switches are to be set.
- T --- The 'T' or trace card provides a fetch-by-fetch program trace, dumping the entire machine status on every fetch cycle. If a 1 is in column 2, the trace will be displayed on the CRT. This card is recommended for debugging programs.

APPENDIX C. AN/UYK-20 EMULATOR INSTRUCTION FORMAT

Format Card Columns

5 6 7 8 9 10 11 12 13 14

RR, RL, opcode , 'f' , ' a ' , ' m '

RI Type 2

5 6 7 8 9 10 11 12

RI Type 1 opcode , 'f' , ' d '

5 6 7 8 9 10 11 12 13 14 15 16 - 20

RK, RX opcode , 'f' , ' a ' , ' m ' , ' y '

Notes:

- 1) All fields are in octal with the exceptions of addresses and the 'y' field which are decimal
- 2) All fields must be zero-filled
- 3) The following field restrictions must be followed:

Field	Range	Base
Opcode	00-76	octal
'f'	0-3	octal
'a'	00-17	octal
'm'	00-17	octal
'd'	000-377	octal
'y'	00000-65535	decimal
addr	00000-65535	decimal

APPENDIX D. SAMPLE DEBUGGER OUTPUT

This appendix provides a sample program output illustrating the Trace option. The debugger is called at the beginning of every instruction fetch, and at the termination of the program. Space has been provided for dumping 48 memory addresses including emulated AN/UYK-20 registers and D-machine registers. Each output line consists of eight regions printed in hexadecimal with a total of eight hex digits (32 bits) per region.

The listing is annotated to indicate the identity of each output cell. A summary of cell definitions (numbering from left to right, top to bottom) follows:

DECIMAL ADDRESS	DESCRIPTION

0 - 15	General Register Stack 1
16 - 31	General Register Stack 2
32	Program Status word (PSW)
33	Breakpoint Register (BREAKPT)
34	Status Register 2 (SR2)
35	NEXTINSTR (next load address)
36	Clocktime
37	Real-Time Clock (RTC)
38	AMPCR
39	A1
40	A2
41	A3
42	MIR
43	BR1
44 - 47	Unused

APPENDIX E. SAMPLE TEST PROGRAMS

The programs listed in this appendix were designed to illustrate how the AN/UYK-20 emulator can be used for developing programs. The first two programs presented are the generation of prime numbers and the solution of simultaneous linear equations by Cramer's Rule. They depict several AN/UYK-20 control structures such as looping, iteration, and condition code testing as well as numerous load, store, and arithmetic operations. The last program performs the Cramer's Rule algorithm and demonstrates input/output routines.

L	C0034	LINEAR EQUATIONS BY CRAMER'S RULE.		
I	I1	X IS RETURNED IN REG 01, Y IN REG 05		
C	00206	FAULT INTERRUPT-EXECUTION ENDS		
C	00214	NOT IMPLEMENTED-EXECUTION ENDS		
C	00222	DIVIDE OVERFLOW - FAULT ENTERED		
D	02048	BOTH EQUATIONS MUST BE IN STD FORM		
D	02049	A (Y) PLUS B (X) EQUALS C		
D	02050	Y COEFF OF 1ST EON		
D	02051	X COEFF OF 1ST EON		
D	02052	CONSTANT OF 1ST EON		
D	02053	Y COEFF OF 2ND EON		
D	02054	X COEFF OF 2ND EON		
D	02055	CONSTANT OF 2ND EON		
C	01030	STORE X COEFF, EON 1, INTO REG 01		
C	01031	STORE Y COEFF, EON 1, INTO REG 03		
C	01032	STORE CONSTANT, EON 1, INTO REG 05		
C	01033	STORE X COEFF, EON 2, INTO REG 11		
C	01034	STORE Y COEFF, EON 2, INTO REG 13		
C	01035	STORE CONSTANT, EON 2, INTO REG 15		
C	01036	MULT LEFT DIAG OF DENOM, RESULT IN 00/01		
C	01037	MULT RT. DIAG OF DENOM, RESULT IN 10/11		
C	01038	SUBTRACT DOUBLE, RESULT OF DENOM IN 00/01		
C	01039	COMPARE DENOM WITH ZERO		
C	01040	JUMP, IF EQUAL (ZERO DETERMINANT)		
C	01041	STORE DOUBLE, DENOM INTO 16/17		
C	01042	LOAD 00 INTO REG 00		
C	01043	RESTORE X COEFF, EON 1, INTO REG 01		
C	01044	RESTORE Y COEFF, EON 1, INTO REG 03		
C	01045	RESTORE CONSTANT OF EON 1 IN REG 05		
C	01046	RESTORE X COEFF OF EON 2 IN REG 11		
C	01047	RESTORE Y COEFF OF EON 2 IN REG 13		
C	01048	RESTORE CONSTANT OF EON 2 IN REG 15		
C	01049	X NUM LEFT DIAG MULT, RESULT IN 00/01		
C	01050	X NUM RT. DIAG MULT, RESULT IN 10/11		
C	01051	X NUM RESULT IN REG 00/01		
C	01052	X RESIDES IN REG 01		
C	01053	Y NUM LEFT DIAG MULT, RESULT REG 04/05		
C	01054	Y NUM RT. DIAG MULT, RESULT REG 04/15		
C	01055	DOUBLE SUBTRACT (FVAL NUM), RESULT 04/05		
C	01056	DIVIDE NUM/DENOM, Y RESIDES IN 05		
C	01057	PRIORITY INTERRUPT, HALT EXECUTION		
C	01058	GOP COMMENCE EXECUTION		
C	01059	MACHINE STATUS TO THE PRINTER		
C	00000000	00000000	00000000	00000000
C	00000001	00000001	00000001	00000001
C	00000002	00000002	00000002	00000002
C	00000003	00000003	00000003	00000003
C	00000004	00000004	00000004	00000004
C	00000005	00000005	00000005	00000005
C	00000006	00000006	00000006	00000006
C	00000007	00000007	00000007	00000007
C	00000008	00000008	00000008	00000008
C	00000009	00000009	00000009	00000009
C	00000010	00000010	00000010	00000010
C	00000011	00000011	00000011	00000011
C	00000012	00000012	00000012	00000012
C	00000013	00000013	00000013	00000013
C	00000014	00000014	00000014	00000014
C	00000015	00000015	00000015	00000015
C	00000016	00000016	00000016	00000016
C	00000017	00000017	00000017	00000017
C	00000018	00000018	00000018	00000018
C	00000019	00000019	00000019	00000019
C	00000020	00000020	00000020	00000020
C	00000021	00000021	00000021	00000021
C	00000022	00000022	00000022	00000022
C	00000023	00000023	00000023	00000023
C	00000024	00000024	00000024	00000024
C	00000025	00000025	00000025	00000025
C	00000026	00000026	00000026	00000026
C	00000027	00000027	00000027	00000027
C	00000028	00000028	00000028	00000028
C	00000029	00000029	00000029	00000029
C	00000030	00000030	00000030	00000030
C	00000031	00000031	00000031	00000031
C	00000032	00000032	00000032	00000032
C	00000033	00000033	00000033	00000033
C	00000034	00000034	00000034	00000034
C	00000035	00000035	00000035	00000035
C	00000036	00000036	00000036	00000036
C	00000037	00000037	00000037	00000037
C	00000038	00000038	00000038	00000038
C	00000039	00000039	00000039	00000039
C	00000040	00000040	00000040	00000040
C	00000041	00000041	00000041	00000041
C	00000042	00000042	00000042	00000042
C	00000043	00000043	00000043	00000043
C	00000044	00000044	00000044	00000044
C	00000045	00000045	00000045	00000045
C	00000046	00000046	00000046	00000046
C	00000047	00000047	00000047	00000047
C	00000048	00000048	00000048	00000048
C	00000049	00000049	00000049	00000049
C	00000050	00000050	00000050	00000050
C	00000051	00000051	00000051	00000051
C	00000052	00000052	00000052	00000052
C	00000053	00000053	00000053	00000053
C	00000054	00000054	00000054	00000054
C	00000055	00000055	00000055	00000055
C	00000056	00000056	00000056	00000056
C	00000057	00000057	00000057	00000057
C	00000058	00000058	00000058	00000058
C	00000059	00000059	00000059	00000059
C	00000060	00000060	00000060	00000060
C	00000061	00000061	00000061	00000061
C	00000062	00000062	00000062	00000062
C	00000063	00000063	00000063	00000063
C	00000064	00000064	00000064	00000064
C	00000065	00000065	00000065	00000065
C	00000066	00000066	00000066	00000066
C	00000067	00000067	00000067	00000067
C	00000068	00000068	00000068	00000068
C	00000069	00000069	00000069	00000069
C	00000070	00000070	00000070	00000070
C	00000071	00000071	00000071	00000071
C	00000072	00000072	00000072	00000072
C	00000073	00000073	00000073	00000073
C	00000074	00000074	00000074	00000074
C	00000075	00000075	00000075	00000075
C	00000076	00000076	00000076	00000076
C	00000077	00000077	00000077	00000077
C	00000078	00000078	00000078	00000078
C	00000079	00000079	00000079	00000079
C	00000080	00000080	00000080	00000080
C	00000081	00000081	00000081	00000081
C	00000082	00000082	00000082	00000082
C	00000083	00000083	00000083	00000083
C	00000084	00000084	00000084	00000084
C	00000085	00000085	00000085	00000085
C	00000086	00000086	00000086	00000086
C	00000087	00000087	00000087	00000087
C	00000088	00000088	00000088	00000088
C	00000089	00000089	00000089	00000089
C	00000090	00000090	00000090	00000090
C	00000091	00000091	00000091	00000091
C	00000092	00000092	00000092	00000092
C	00000093	00000093	00000093	00000093
C	00000094	00000094	00000094	00000094
C	00000095	00000095	00000095	00000095
C	00000096	00000096	00000096	00000096
C	00000097	00000097	00000097	00000097
C	00000098	00000098	00000098	00000098
C	00000099	00000099	00000099	00000099
C	00000100	00000100	00000100	00000100
C	00000101	00000101	00000101	00000101
C	00000102	00000102	00000102	00000102
C	00000103	00000103	00000103	00000103
C	00000104	00000104	00000104	00000104
C	00000105	00000105	00000105	00000105
C	00000106	00000106	00000106	00000106
C	00000107	00000107	00000107	00000107
C	00000108	00000108	00000108	00000108
C	00000109	00000109	00000109	00000109
C	00000110	00000110	00000110	00000110
C	00000111	00000111	00000111	00000111
C	00000112	00000112	00000112	00000112
C	00000113	00000113	00000113	00000113
C	00000114	00000114	00000114	00000114
C	00000115	00000115	00000115	00000115
C	00000116	00000116	00000116	00000116
C	00000117	00000117	00000117	00000117
C	00000118	00000118	00000118	00000118
C	00000119	00000119	00000119	00000119
C	00000120	00000120	00000120	00000120
C	00000121	00000121	00000121	00000121
C	00000122	00000122	00000122	00000122
C	00000123	00000123	00000123	00000123
C	00000124	00000124	00000124	00000124
C	00000125	00000125	00000125	00000125
C	00000126	00000126	00000126	00000126
C	00000127	00000127	00000127	00000127
C	00000128	00000128	00000128	00000128
C	00000129	00000129	00000129	00000129
C	00000130	00000130	00000130	00000130
C	00000131	00000131	00000131	00000131
C	00000132	00000132	00000132	00000132
C	00000133	00000133	00000133	00000133
C	00000134	00000134	00000134	00000134
C	00000135	00000135	00000135	00000135
C	00000136	00000136	00000136	00000136
C	00000137	00000137	00000137	00000137
C	00000138	00000138	00000138	00000138
C	00000139	00000139	00000139	00000139
C	00000140	00000140	00000140	00000140
C	00000141	00000141	00000141	00000141
C	00000142	00000142	00000142	00000142
C	00000143	00000143	00000143	00000143
C	00000144	00000144	00000144	00000144
C	00000145	00000145	00000145	00000145
C	00000146	00000146	00000146	00000146


```

P 00030
L 00230 FAULT INTERRUPT--EXECUTION ENDS *
C 00210 NOT IMPLEMENTED--EXECUTION ENDS *
C 00220 DIVIDE OVERFLOW - FAULT ENTERED!
I2 30 17650 10CM FOR 20 BUFFERS FROM CARD HEADER
I2 31 04076 10CM FOR 6 BUFFERS FROM CARD READER
I2 32 16758
I2 03 05120
I2 04 16705
I2 05 08076
I2 06 17655
I2 07 10240
I2 08 12336
I2 11 C0040
I2 15 00C30
D 02048 00C30
D 02049 C0030
D 02050 00C31
D 02C31 00C31
D 02032 00C33
D 02033 00031
D 02034 65545
D 02055 65545
63+0+13+01
03+0+13+05
12+1+00+17
35+0+07+00
12+1+02+17
35+0+03+00
01+2+12+00+01320
01+2+11+00+10240
15+1+10+11
02+0+12+11
45+1+375
01+2+14+00+04076
01+2+15+00+00C20
01+2+11+00+10240
05+1+15+14
15+1+15+11
02+0+13+11
45+1+374
22+2+11+00+00C26
01+2+13+00+00C40
02+0+13+11
45+1+356
12+1+15+17
35+0+03+00

```

BOTH EQUATIONS MUST BE IN STD FORM
A (Y) PLUS B (X) EQUALS C
Y COEFF OF 1ST EON
X COEFF OF 1ST EON
CONSTANT OF 1ST EON
Y COEFF OF 2ND EON
X COEFF OF 2ND EON
CONSTANT OF 2ND EON
LOAD 1 INTO REG. 12
LOAD S91 WITH REG. 12
STORE DOUBLE INTO 10CM
INPUT 14 BUFFERS FROM CARD READER
STORE DOUBLE INTO 10CM
INPUT 6 BUFFERS FROM THE CARD READER
INITIALIZE BUFFER WORDS COUNT (20 PRT BUFFERS)
INITIALIZE OUTPUT BUFFER ADDR
STORE (RA) INTO Y* AND INDEX BY 1 (STORE SPACES)
DECREMENT BUFFER COUNTER
COUNTER EQUAL ZERO
INITIALIZE BUFFER ADDRESS OF INPUT
BUFFER COUNT
INITIALIZE DESTINATION BUFFER ADDR
LOAD AND INDEX BY 1
STORE RA INTO Y* AND INDEX Y*
DECREMENT COUNTER
COUNTER EQUAL ZERO
ADD 26 TO BUFFER ADDR
RESET - BUFFER WORD COUNT
DECREMENT NEXT COUNTER (NO. OF BUFFERS)
COUNTER EQUAL ZERO
STORE DOUBLE INTO 10CM
OUTPUT 14 BUFFERS TO PRT


```

63+0+13+01
03+0+13+05
01+2+11+00+00076
01+2+12+00+00030
01+2+13+00+00035
01+2+14+00+00035
01+2+15+00+00120
15+1+10+11
02+0+12+11
45+1+375
01+2+11+00+00076
05+1+15+14
15+1+15+11
02+0+13+11
45+1+374
22+2+11+00+00026
01+2+13+00+00040
02+0+13+11
45+1+356
63+0+13+00
03+0+13+05
01+3+01+00+00030
01+3+03+00+00031
01+3+05+00+00032
01+3+11+00+00033
01+3+13+00+00034
01+3+15+00+00035
26+0+13+03
21+0+00+10
25+3+00+17+02040
44+1+052
12+3+07+06+00014
01+2+02+00+00030
01+3+01+00+00030
01+3+03+00+00031
01+3+05+00+00032
01+3+11+00+00033
01+3+13+00+00034
01+3+15+00+00035
26+0+00+15
26+0+13+05
21+0+00+10
27+0+00+17
26+0+00+13
26+0+10+03
21+0+03+14
27+0+03+17

***RE-ENTRY POINT FOR REPETITIVE EXECUTION***
LOAD SRI WITH A 1 FROM REG 13
INITIALIZE NEXT OUTPUT BUFFER ADDRESS
INITIALIZE NEXT BUFFER WORD COUNT (5 PRT BUFFERS)
BUFFER COUNT
INITIALIZE BUFFER ADDR OF SECOND INPUT BUFFER
STORE (RA) INTO Y* AND INDEX BY 1 (STORE SPACES)
DECREMENT GUFER COUNTER
COUNTER EQUAL ZERO
REINITIALIZE BUFFER ADDR IN REG 9
LOAD AND INDEX BY J
STORE RA INTO Y* AND INDEX Y*
DECREMENT COUNTER
COUNTER EQUAL ZERO
ADD 26 TO BUFFER ADDR
RESET BUFFER WORD COUNT
DECREMENT NEXT COUNTER (NO. OF BUFFERS)
COUNTER EQUAL ZERO
LOAD REG 13 WITH 0
LOAD SRI WITH 0
***CRAMER'S RULE ALGORITHM*** STORE X OF EON 1
STORE Y COEFF, EON 1, INTO REG 03
STORE CONSTANT, EON 1, INTO REG 05
STORE X COEFF, EON 2, INTO REG 11
STORE X COEFF, EON 2, INTO REG 13
STORE CONSTANT, EON 2, INTO REG 15
NUM LEFT DIAG OF DENOM, RESULT IN 00/01
MULT RT, DIAG OF DENOM, RESULT IN 10/11
SUBTRACT DOUBLE, RESULT OF DENOM IN 00/01
COMPARE DENOM WITH ZERO
JUMP, IF EQUAL (ZERO DETERMINANT)
STORE DOUBLE, DENOM INTO 16/17
LOAD 00 INTO REG 00
RESTORE Y COEFF, EON 1, INTO REG 01
RESTORE X COEFF, EON 1, INTO REG 03
RESTORE CONSTANT OF EON 1 IN REG 05
RESTORE Y COEFF OF EON 2 IN REG 11
RESTORE X COEFF OF EON 2 IN REG 13
RESTORE CONSTANT OF EON 2 IN REG 15
X NUM LEFT DIAG MULT, RESULT IN 00/01
X NUM RT, 01AG MULT, RESULT IN 10/11
X NUM RESULT IN REG 00/01
X RESIDES IN REG 01
Y NUM LEFT DIAG MULT, RESULT REG 04/05
Y NUM RT, DIAG MULT, RESULT REG 14/15
DOUBLE SUBTRACT (EVAL NUM), RESULT 04/05
DIVIDE NUM/DENOM, Y RESIDES IN 05

```



```

01:2:07:00:16359
63:0:03:00
63:3:09:12
1C:3:03:07:00030
44:1:023
63:0:07:00
62:0:07:01
40:1:371
01:2:07:00:16633
63:0:04:00
63:3:03:12
1C:3:01:07:00070
44:1:023
63:0:04:00
62:0:07:01
40:1:371
63:0:15:01
03:0:15:05
12:1:04:17
35:0:03:00
03:0:05:00
63:0:15:01
03:0:15:05
2C:2:11:00:00178
01:2:13:00:00040
15:1:15:14
15:1:15:11
02:0:13:11
45:1:374
12:1:04:17
35:0:03:00
03:0:05:00

***INT TO BCL CONVERSION*** TWICE BUFFER ADDR PLUS 1
LIT LOAD, C INTO REG 0
LIT DIVIDE, REG 0/1 BY 10
BYTE STORE, REG 7 MUST CONTAIN TWICE ADDR
LOCAL JUMP EQUAL (ZERO QUOTIENT)
LIT LOAD, C INTO REG 0
LIT SUBTRACT, 1 FROM REG 7
LOCAL JUMP
LOAD CONSTANT, TWICE ADDR PLUS 1 IN REG. 7
LIT LOAD, C INTO REG 4
LIT DIVIDE, REG 4/5 BY 10
BYTE JUMP
JUMP EQUAL, CHECK FOR ZERO QUOTIENT
LIT LOAD, C INTO REG 4
LIT SUBTRACT, 1 FROM REG 7
LOCAL JUMP
LOAD REG 13 WITH A 1
LOAD SR1 WITH A 1
STORE DOUBLE INTO 10CM
DUMP 5 BUFFERS TO PRI
HALT

***NO SOLUTION CASE***
LOAD SR1 WITH A 1
RECOMPUTE OUTPUT BUFFER ADDR FOR *NO SOLUTION*
REINITIALIZE COUNTER
LOAD AND INDEX BY 1
STORE RA INTO Y* AND INDEX Y*
DECREMENT COUNTER
COUNTER EQUAL ZERO
STORE DOUBLE INTO 10CM
DUMP 5 BUFFERS TO PRI
HALT

```


THIS IS A DEMONSTRATION PROGRAM OF THE AN/JYK20 EMULATOR.
THE PROGRAM SOLVES TWO SIMULTANEOUS EQUATIONS BY CRAMER'S RULE.

THE INPUT COEFFICIENT VALUES AND CONSTANTS FOR EACH EQUATION MUST BE INSERTED
USING LOADER CONTROL CARDS IN THE FOLLOWING LOCATIONS

1ST EQUATION. A1 IN LOCATION 2050 D.
B1 IN LOCATION 2051 D.
CONSTANT IV LOCATION 2052 D.

2ND EQUATION. A2 IN LOCATION 2053 D.
B2 IN LOCATION 2054 D.
CONSTANT IV LOCATION 2055 D.

THE RESULT IS.
X > 2

Y > 1
TO CHANGE VARIABLES INSERT LOADER JCL HERE, OTHERWISE EXIT
11 00C30 REINITIALIZE BUFFER WORD COUNT FOR BUFFER INIT.
12 02053 Y COEFF OF 2ND EQUATION
13 00C31 X COEFF OF 2ND EQUATION
14 02054 Y COEFF OF 1ST EQUATION
15 02055 CONSTANT OF 2ND EQUATION
16 00C31 RE-EXECUTE PROGRAM AT ADDR 1055 DECIMAL

THE RESULT IS.
X > 1
NO SOLUTION

Y > 1
TO CHANGE VARIABLES INSERT LOADER JCL HERE, OTHERWISE EXIT
E END EXECUTION

APPENDIX F. EMULATOR LISTING

This appendix provides a listing of the TRANSLANG assembler output of the AN/UYK-20 emulation. A source file copy of the emulator exists on disk as well as on cards. A microinstruction object file is also maintained on disk.

The listing is divided into four sections. The left most section contains the microinstruction address composed of four hexadecimal digits followed by a 56-bit microinstruction created from a TRANSLANG instruction. The center section contains the TRANSLANG source which includes labels, an instruction, and/or a comment field. The final number printed on the right most side of the listing is the sequence number of the TRANSLANG source statement. This number, printed in decimal, is created by a Burroughs software utility program called CARD-LIST. This number must be used when editing source programs on disk.

[illegible]

0C7A	1C86	C002	001C	1CFC	0C7A	SET GC2 WHEN GC2 THEN NOT 0 = MAR2	00239C00	D
0C7B	9809	08C0	0030	1CFC	0C7B	IF SAI	0C294C00	D
0C7C	9F0A	08C0	0030	1CFC	0C7C	WHEN SAI THEN 01 SET INT	0C294C00	D
0C7D	0809	00C0	0C3C	1CFC	0C7D	IF INT	0C294C00	D
0C7E	0808	00C0	0C30	1CFC	0C7E	WHEN INT THEN STEP	0C294C00	C
0C7F	88C9	08C0	0C30	1CFC	0C7F	BEY: MR2: IF ROC	0C294C00	D
0C80	8EC8	0C42	0030	1CFC	0C80	WHEN ROC THEN NOT 01 RESET GC2	0C294C00	D
0C81	882F	0C00	0030	1CFC	0C81	IF ABT THEN JUMP ELSE RETN	0C294C00	D
0C82	9809	08C0	0C30	1CFC	0C82	IF SAI	0C294C00	D
0C83	9C28	08C0	0C30	1CFC	0C83	WHEN SAI THEN 01 JUMP	0C294C00	D
0C84	4809	2001	200C	00F0	0C84	LIT L = A2	0C254C00	D
0C85	0860	00C0	0C3C	1CFC	0C85	COMP 16 = SARI 6 = LIT	0C254C00	D
0C86	4809	CC52	0030	00F0	0C86	OR B = B	0C254C00	D
0C87	4820	00C0	0030	00F0	0C87	JUMP	0C254C00	D
0C88	49C9	00C0	0C30	00F0	0C88	SET LC1	0C269C00	D
0C89	4809	00C0	0C30	00F0	0C89	0 = MIR	0C269C00	D
0C9A	4809	0C00	0030	1CFC	0C9A	LC1R	0C270000	D
0C8B	5030	00C0	0C30	00F0	0C8B	3 = LIT: COMP 4 = SARI	0C270000	D
0C8C	4809	A0C1	4C30	00F0	0C8C	A1 L = A1	0C272C00	D
0C8D	4809	A0C0	8F3C	00F0	0C8D	A1 R = B61	0C274C00	D
0C8E	4809	0C41	0C32	00F0	0C8E	B L = MIR: INC	0C275C00	D
0C8F	540E	A0C1	4C30	00F0	0C8F	IF NOT COW THEN A1 L = A1: STEP ELSE SKIP	0C276C00	D
0C90	086C	00C0	0030	00F0	0C90	BRANCH TO TOP OF LOOP	0C280C00	D
0C91	2819	00C0	0030	00F0	0C91	IF LC1 THEN SKIP	0C281C00	D
0C92	01C0	00C0	0C30	00F0	0C92	PACKEND - 1 = MPCR	0C282C00	D
0C93	4809	0C45	001C	00F0	0C93	ONLY D1: IF THE ROUTINE	0C283C00	D
0C94	4809	00C0	0C3C	1CFC	0C94	PREPARE MAR: READ NEXT 4 DIGITS	0C284C00	D
0C95	AC08	0C40	4C30	00F0	0C95	IF B: NOW CONTAINS LOW ORDER 4 DIGITS	0C285C00	D
0C96	0890	00C0	0C30	00F0	0C96	IF AN 8 DIGIT NUMBER	0C286C00	D
0C97	4820	00C0	0C30	00F0	0C97	WHEN ROC THEN B = A1	0C287C00	D
						NEXT4 - 1 = MPCR	0C288C00	D
						JUMP	0C289C00	D
						PACKEND:	0C290C00	C
						RETURN TO CALLING ROUTINE WITH PACKED	0C291C00	D
						NUMBER IN B REGISTER	0C292C00	D
							0C293C00	D
						THIS ROUTINE WILL CONVERT DECIMAL	0C294C00	C
						NUMBERS INTO THEIR OCTAL EQUIVALENTS.	0C295C00	D
						THIS ROUTINE REQUIRES A PACKED DECIMAL	0C296C00	D
						NUMBER PASSED VIA THE D REGISTER. THE	0C297C00	D


```

%098 4809 0C43 0C3C 00FC
%099 4809 0C0C 003C 00FC
%09A 4809 00C0 0031 00FC
%09B 00C0 00C3 0070 00C0

%09C 4809 4800 9C3C 00FC
%09D 4809 00C0 0C30 00C0
%09E 4809 48C1 4C70 00FC
%09F 48C9 4C41 1830 00FC
%0A0 70C0 0000 0030 00C0
%0A1 4809 4C41 0832 00FC
%0A2 3000 00C0 0C30 00C0
%0A3 4809 4C43 0C70 00FC
%0A4 3C19 4800 9C3C 00FC
%0A5 0980 00C3 0030 0040
%0A6 300C 00C0 0030 003C
%0A7 4809 4C40 0830 00FC
%0A8 4820 00C3 0030 00FC

%0A9 051C 0000 0030 006C
%0AA 4809 0C40 1030 00FC
%0AB 4809 20C3 001C 00FC
%0AC 0700 00C3 0030 00C0
%0AD 046C 00C3 0C30 0060
%0AE 4809 0C43 4C30 00FC
%0AF 0870 00C3 00C0 0060
%0B0 4809 48C0 2030 00FC
%0B1 097C 0000 0000 0060
%0B2 4809 0C40 0C30 00FC
%0B3 4809 0C12 003C 00FC
%0B4 5808 00C0 003C 00FC
%0B5 010C 0000 0070 0040
%0B6 4809 0C03 001C 00FC
%0B7 05EC 0003 0070 0040

%0B8 4809 2003 201C 0060
%0B9 0230 00C3 0030 0060
%0BA 0460 00C0 0030 0060
%0BB 4809 0C43 001C 00FC
%0BC 0810 00C3 00C0 0060
%0BD 4809 0C45 0030 00FC
%0BE 4809 0C03 001C 00FC
%0BF 05E0 00C3 0030 0040

%0C0 4809 00C0 9C3C 00FC
%0C1 4809 00C0 0C30 00C0
%0C2 4809 00C0 0031 00FC
%0C3 00C0 00C3 0070 00C0

%0C4 4809 4800 9C3C 00FC
%0C5 4809 00C0 0C30 00C0
%0C6 4809 00C0 0031 00FC
%0C7 00C0 00C3 0070 00C0

%0C8 4809 48C1 4C70 00FC
%0C9 48C9 4C41 1830 00FC
%0CA 70C0 0000 0030 00C0
%0CB 4809 4C41 0832 00FC
%0CC 3000 00C0 0C30 00C0
%0CD 4809 4C43 0C70 00FC
%0CE 3C19 4800 9C3C 00FC
%0CF 0980 00C3 0030 0040
%0D0 300C 00C0 0030 003C
%0D1 4809 4C40 0830 00FC
%0D2 4820 00C3 0030 00FC

%0D3 051C 0000 0030 006C
%0D4 4809 0C40 1030 00FC
%0D5 4809 20C3 001C 00FC
%0D6 0700 00C3 0030 00C0
%0D7 046C 00C3 0C30 0060
%0D8 4809 0C43 4C30 00FC
%0D9 0870 00C3 00C0 0060
%0DA 4809 48C0 2030 00FC
%0DB 097C 0000 0000 0060
%0DC 4809 0C40 0C30 00FC
%0DD 4809 0C12 003C 00FC
%0DE 5808 00C0 003C 00FC
%0DF 010C 0000 0070 0040
%0E0 4809 0C03 001C 00FC
%0E1 05EC 0003 0070 0040

%0E2 4809 2003 201C 0060
%0E3 0230 00C3 0030 0060
%0E4 0460 00C0 0030 0060
%0E5 4809 0C43 001C 00FC
%0E6 0810 00C3 00C0 0060
%0E7 4809 0C45 0030 00FC
%0E8 4809 0C03 001C 00FC
%0E9 05E0 00C3 0030 0040

%0EA 4809 00C0 9C3C 00FC
%0EB 4809 00C0 0C30 00C0
%0EC 4809 00C0 0031 00FC
%0ED 00C0 00C3 0070 00C0

%0EE 4809 48C1 4C70 00FC
%0EF 48C9 4C41 1830 00FC
%0F0 70C0 0000 0030 00C0
%0F1 4809 4C41 0832 00FC
%0F2 3000 00C0 0C30 00C0
%0F3 4809 4C43 0C70 00FC
%0F4 3C19 4800 9C3C 00FC
%0F5 0980 00C3 0030 0040
%0F6 300C 00C0 0030 003C
%0F7 4809 4C40 0830 00FC
%0F8 4820 00C3 0030 00FC

```

```

%0F9 051C 0000 0030 006C
%0FA 4809 0C40 1030 00FC
%0FB 4809 20C3 001C 00FC
%0FC 0700 00C3 0030 00C0
%0FD 046C 00C3 0C30 0060
%0FE 4809 0C43 4C30 00FC
%0FF 0870 00C3 00C0 0060
%100 4809 48C0 2030 00FC
%101 097C 0000 0000 0060
%102 4809 0C40 0C30 00FC
%103 4809 0C12 003C 00FC
%104 5808 00C0 003C 00FC
%105 010C 0000 0070 0040
%106 4809 0C03 001C 00FC
%107 05EC 0003 0070 0040

%108 4809 2003 201C 0060
%109 0230 00C3 0030 0060
%10A 0460 00C0 0030 0060
%10B 4809 0C43 001C 00FC
%10C 0810 00C3 00C0 0060
%10D 4809 0C45 0030 00FC
%10E 4809 0C03 001C 00FC
%10F 05E0 00C3 0030 0040

%110 4809 00C0 9C3C 00FC
%111 4809 00C0 0C30 00C0
%112 4809 00C0 0031 00FC
%113 00C0 00C3 0070 00C0

%114 4809 48C1 4C70 00FC
%115 48C9 4C41 1830 00FC
%116 70C0 0000 0030 00C0
%117 4809 4C41 0832 00FC
%118 3000 00C0 0C30 00C0
%119 4809 4C43 0C70 00FC
%11A 3C19 4800 9C3C 00FC
%11B 0980 00C3 0030 0040
%11C 300C 00C0 0030 003C
%11D 4809 4C40 0830 00FC
%11E 4820 00C3 0030 00FC

```

```

%11F 051C 0000 0030 006C
%120 4809 0C40 1030 00FC
%121 4809 20C3 001C 00FC
%122 0700 00C3 0030 00C0
%123 046C 00C3 0C30 0060
%124 4809 0C43 4C30 00FC
%125 0870 00C3 00C0 0060
%126 4809 48C0 2030 00FC
%127 097C 0000 0000 0060
%128 4809 0C40 0C30 00FC
%129 4809 0C12 003C 00FC
%12A 5808 00C0 003C 00FC
%12B 010C 0000 0070 0040
%12C 4809 0C03 001C 00FC
%12D 05EC 0003 0070 0040

%12E 4809 2003 201C 0060
%12F 0230 00C3 0030 0060
%130 0460 00C0 0030 0060
%131 4809 0C43 001C 00FC
%132 0810 00C3 00C0 0060
%133 4809 0C45 0030 00FC
%134 4809 0C03 001C 00FC
%135 05E0 00C3 0030 0040

%136 4809 00C0 9C3C 00FC
%137 4809 00C0 0C30 00C0
%138 4809 00C0 0031 00FC
%139 00C0 00C3 0070 00C0

%13A 4809 48C1 4C70 00FC
%13B 48C9 4C41 1830 00FC
%13C 70C0 0000 0030 00C0
%13D 4809 4C41 0832 00FC
%13E 3000 00C0 0C30 00C0
%13F 4809 4C43 0C70 00FC
%140 3C19 4800 9C3C 00FC
%141 0980 00C3 0030 0040
%142 300C 00C0 0030 003C
%143 4809 4C40 0830 00FC
%144 4820 00C3 0030 00FC

```

```

%145 051C 0000 0030 006C
%146 4809 0C40 1030 00FC
%147 4809 20C3 001C 00FC
%148 0700 00C3 0030 00C0
%149 046C 00C3 0C30 0060
%14A 4809 0C43 4C30 00FC
%14B 0870 00C3 00C0 0060
%14C 4809 48C0 2030 00FC
%14D 097C 0000 0000 0060
%14E 4809 0C40 0C30 00FC
%14F 4809 0C12 003C 00FC
%150 5808 00C0 003C 00FC
%151 010C 0000 0070 0040
%152 4809 0C03 001C 00FC
%153 05EC 0003 0070 0040

%154 4809 2003 201C 0060
%155 0230 00C3 0030 0060
%156 0460 00C0 0030 0060
%157 4809 0C43 001C 00FC
%158 0810 00C3 00C0 0060
%159 4809 0C45 0030 00FC
%15A 4809 0C03 001C 00FC
%15B 05E0 00C3 0030 0040

%15C 4809 00C0 9C3C 00FC
%15D 4809 00C0 0C30 00C0
%15E 4809 00C0 0031 00FC
%15F 00C0 00C3 0070 00C0

%160 4809 48C1 4C70 00FC
%161 48C9 4C41 1830 00FC
%162 70C0 0000 0030 00C0
%163 4809 4C41 0832 00FC
%164 3000 00C0 0C30 00C0
%165 4809 4C43 0C70 00FC
%166 3C19 4800 9C3C 00FC
%167 0980 00C3 0030 0040
%168 300C 00C0 0030 003C
%169 4809 4C40 0830 00FC
%16A 4820 00C3 0030 00FC

```

```

%16B 051C 0000 0030 006C
%16C 4809 0C40 1030 00FC
%16D 4809 20C3 001C 00FC
%16E 0700 00C3 0030 00C0
%16F 046C 00C3 0C30 0060
%170 4809 0C43 4C30 00FC
%171 0870 00C3 00C0 0060
%172 4809 48C0 2030 00FC
%173 097C 0000 0000 0060
%174 4809 0C40 0C30 00FC
%175 4809 0C12 003C 00FC
%176 5808 00C0 003C 00FC
%177 010C 0000 0070 0040
%178 4809 0C03 001C 00FC
%179 05EC 0003 0070 0040

%17A 4809 2003 201C 0060
%17B 0230 00C3 0030 0060
%17C 0460 00C0 0030 0060
%17D 4809 0C43 001C 00FC
%17E 0810 00C3 00C0 0060
%17F 4809 0C45 0030 00FC
%180 4809 0C03 001C 00FC
%181 05E0 00C3 0030 0040

%182 4809 00C0 9C3C 00FC
%183 4809 00C0 0C30 00C0
%184 4809 00C0 0031 00FC
%185 00C0 00C3 0070 00C0

%186 4809 48C1 4C70 00FC
%187 48C9 4C41 1830 00FC
%188 70C0 0000 0030 00C0
%189 4809 4C41 0832 00FC
%18A 3000 00C0 0C30 00C0
%18B 4809 4C43 0C70 00FC
%18C 3C19 4800 9C3C 00FC
%18D 0980 00C3 0030 0040
%18E 300C 00C0 0030 003C
%18F 4809 4C40 0830 00FC
%190 4820 00C3 0030 00FC

```



```

00C0 004C 0009 0000 0060
00C1 4809 0041 0020 0030
00C2 0000 0000 0020 0030
00C3 4809 0040 0000 0000
00C4 4809 000E 0020 0000
00C5 4809 0041 0020 0000
00C6 8000 0000 0020 0030
00C7 4809 0041 0020 0000
00C8 0000 0000 0000 0030
00C9 4809 2000 001C 0000
00CA 0780 0000 0000 0000
00CB 004C 0000 0000 0000
00CC 4809 0041 0020 0000
00CD 0000 0000 0000 0020
00CE 4809 0040 0000 0000
00CF 0000 0000 0000 0000
00D0 0000 0000 0000 0000
00D1 4809 0000 0000 0000
00D2 4809 0000 0000 0000
00D3 0000 0000 0000 0000
00D4 4809 0041 0020 0000
00D5 0700 0000 0000 0000
00D6 4809 2000 001C 0000
00D7 004C 0000 0000 0000
00D8 4809 0000 0000 0000
00D9 4809 0040 0000 0000
00DA 4809 0040 0000 0000
00DB 4809 0040 0000 0000
00DC 4809 0040 0000 0000
00DD 0000 0000 0000 0000
00DE 4809 0000 0000 0000
00DF 4809 0040 0000 0000
00E0 0000 0000 0000 0000
00E1 4809 0000 0000 0000
00E2 0000 0000 0000 0000
00E3 4809 2000 001C 0000
00E4 0000 0000 0000 0000
00E5 004C 0000 0000 0000
00E6 4809 0040 0000 0000
00E7 0000 0000 0000 0000
00E8 4809 0040 0000 0000
00E9 0000 0000 0000 0000
00EA 0000 0000 0000 0000
00EB 0000 0000 0000 0000
00EC 0000 0000 0000 0000
00ED 0000 0000 0000 0000
00EE 4809 0000 0000 0000
00EF 8000 0000 0000 0000
00F0 4809 0000 0000 0000
00F1 0000 0000 0000 0000

```

INPUT - 1 = CPCR
 COMP 0 = SAR
 COMP 8 = SAR
 B R = 0 * A1
 A1 - 1 = B
 B L = B
 COMP 4 = SAR
 B L = B R1 * MAR
 COMP 8 = SAR
 LIT = MAR2
 CAR05X8 = LIT
 INPUT - 1 = CPCR
 B L = B
 COMP 16 = SAR
 PACKED = CPCR
 DECOCT - 1 = CPCR
 ASR
 BHAR R = A1
 B = SAR
 A1 * B L = B R1
 COMP 8 = SAR
 LIT = MAR2
 INPUT - 1 = CPCR
 ASR
 BHAR R = MAR2
 B = SAR
 B = MIR
 OUT-1 = HPCR

BREAKPOINT:
 BEX
 B L = A1
 COMP 8 = SAR
 A1 R = A1
 24 = SAR
 LIT = MAR2
 PSW = LIT
 INPUT - 1 = CPCR
 A1 EOL LIT
 41 = LIT
 IF FALSE THEN A1 EOL
 BRKREAD - 1 = HPCR
 54 = LIT
 IF FALSE THEN SKIP
 BRKWRITE - 1 = HPCR
 BRK00TH - 1 = HPCR

BRKREAD:
 1 L = A1
 COMP 20 = SAR
 A1 OR B = MIR
 OUTPUT1 - 1 = CPCR

* STORED IN THE DESIRED GENERAL REGISTER
 * REREAD COL. 1 - 4
 * ISOLATE COLUMN 2
 * B IS NOW OXGEN REG. NO., 13 OR 1 (NO. 2)
 * ADDRESS OF GENERAL REGISTER STACK
 * MULTIPLY BY 16
 * STORE BASE ADDR OF GEN REG STACK
 * SHIFT TO PROPER POS. FOR BR1
 * LOAD ADDR OF CARL COL 5-6
 * READ CARO COL. 5-8
 * ISOLATE CARD COL 7-8
 * A1 CONTAINS COL 7-8 (GEN REG NO.)
 * JUMP TO 2ND LINE IN ROUTINE (4 DIGIT NO. 00374C00)
 * B HAS OCTAL VALUE OF GEN REG NUMBER
 * SET MAR1 AS MOST RECENTLY REFERENCED
 * MOVE BASE ADDR TO A1 FROM BR1
 * SHIFT OHAR TO ISOLATE BR1
 * (CREATE GEN REG ADDRESS + OFFSET)
 * ADDRESS OF DATA
 * READ IN DATA
 * SET MAR1 AS MOST RECENTLY REFERENCED
 * LOAD GEN REG. ADDR INTO MAR2
 * SHIFT TO ISOLATE BR1
 * B HAS OCTAL VALUE OF DATA
 * WRITE DATA FROM COL. 13-20 INTO
 * SPECIFIED GENERAL REGISTER
 * SET UP BREAKPOINT REGISTER AND SET
 * STATUS BITS
 * FILL B WITH CARD COL 1-4 (FROM SW1)
 * ISOLATE THE R/M/B CHARACTER
 * ISOLATE COLUMN 2
 * WRITE PSW INTO B
 * INPUT FROM MEMORY
 * CHECK FOR CHARACTER IN:
 * LIT1 SKIP
 * JUMP TO BREAKPOINT READ SUBFUNCTION
 * CHECK FOR 1st CHARACTER
 * JUMP TO BREAKPOINT WRITE SUBFUNCTION
 * DEFAULTS TO BREAKPOINT BOTH (R/B)
 * THIS ROUTINE SETS UP THE BREAKPOINT
 * REGISTER AND SETS THE READ STATUS BITS
 * SET BIT # 20 OF PSW REG
 * WRITE PSW INTO MEMORY

OPCODE	OP	OPN	OPND	OPND2	OPND3	OPND4	OPND5	OPND6	OPND7	OPND8	OPND9	OPND10	OPND11	OPND12	OPND13	OPND14	OPND15	OPND16	OPND17	OPND18	OPND19	OPND20	OPND21	OPND22	OPND23	OPND24	OPND25	OPND26	OPND27	OPND28	OPND29	OPND30	OPND31	OPND32	OPND33	OPND34	OPND35	OPND36	OPND37	OPND38	OPND39	OPND40	OPND41	OPND42	OPND43	OPND44	OPND45	OPND46	OPND47	OPND48	OPND49	OPND50	OPND51	OPND52	OPND53	OPND54	OPND55	OPND56	OPND57	OPND58	OPND59	OPND60	OPND61	OPND62	OPND63	OPND64	OPND65	OPND66	OPND67	OPND68	OPND69	OPND70	OPND71	OPND72	OPND73	OPND74	OPND75	OPND76	OPND77	OPND78	OPND79	OPND80	OPND81	OPND82	OPND83	OPND84	OPND85	OPND86	OPND87	OPND88	OPND89	OPND90	OPND91	OPND92	OPND93	OPND94	OPND95	OPND96	OPND97	OPND98	OPND99	OPND100	OPND101	OPND102	OPND103	OPND104	OPND105	OPND106	OPND107	OPND108	OPND109	OPND110	OPND111	OPND112	OPND113	OPND114	OPND115	OPND116	OPND117	OPND118	OPND119	OPND120	OPND121	OPND122	OPND123	OPND124	OPND125	OPND126	OPND127	OPND128	OPND129	OPND130	OPND131	OPND132	OPND133	OPND134	OPND135	OPND136	OPND137	OPND138	OPND139	OPND140	OPND141	OPND142	OPND143	OPND144	OPND145	OPND146	OPND147	OPND148	OPND149	OPND150	OPND151	OPND152	OPND153	OPND154	OPND155	OPND156	OPND157	OPND158	OPND159	OPND160	OPND161	OPND162	OPND163	OPND164	OPND165	OPND166	OPND167	OPND168	OPND169	OPND170	OPND171	OPND172	OPND173	OPND174	OPND175	OPND176	OPND177	OPND178	OPND179	OPND180	OPND181	OPND182	OPND183	OPND184	OPND185	OPND186	OPND187	OPND188	OPND189	OPND190	OPND191	OPND192	OPND193	OPND194	OPND195	OPND196	OPND197	OPND198	OPND199	OPND200	OPND201	OPND202	OPND203	OPND204	OPND205	OPND206	OPND207	OPND208	OPND209	OPND210	OPND211	OPND212	OPND213	OPND214	OPND215	OPND216	OPND217	OPND218	OPND219	OPND220	OPND221	OPND222	OPND223	OPND224	OPND225	OPND226	OPND227	OPND228	OPND229	OPND230	OPND231	OPND232	OPND233	OPND234	OPND235	OPND236	OPND237	OPND238	OPND239	OPND240	OPND241	OPND242	OPND243	OPND244	OPND245	OPND246	OPND247	OPND248	OPND249	OPND250	OPND251	OPND252	OPND253	OPND254	OPND255	OPND256	OPND257	OPND258	OPND259	OPND260	OPND261	OPND262	OPND263	OPND264	OPND265	OPND266	OPND267	OPND268	OPND269	OPND270	OPND271	OPND272	OPND273	OPND274	OPND275	OPND276	OPND277	OPND278	OPND279	OPND280	OPND281	OPND282	OPND283	OPND284	OPND285	OPND286	OPND287	OPND288	OPND289	OPND290	OPND291	OPND292	OPND293	OPND294	OPND295	OPND296	OPND297	OPND298	OPND299	OPND300	OPND301	OPND302	OPND303	OPND304	OPND305	OPND306	OPND307	OPND308	OPND309	OPND310	OPND311	OPND312	OPND313	OPND314	OPND315	OPND316	OPND317	OPND318	OPND319	OPND320	OPND321	OPND322	OPND323	OPND324	OPND325	OPND326	OPND327	OPND328	OPND329	OPND330	OPND331	OPND332	OPND333	OPND334	OPND335	OPND336	OPND337	OPND338	OPND339	OPND340	OPND341	OPND342	OPND343	OPND344	OPND345	OPND346	OPND347	OPND348	OPND349	OPND350	OPND351	OPND352	OPND353	OPND354	OPND355	OPND356	OPND357	OPND358	OPND359	OPND360	OPND361	OPND362	OPND363	OPND364	OPND365	OPND366	OPND367	OPND368	OPND369	OPND370	OPND371	OPND372	OPND373	OPND374	OPND375	OPND376	OPND377	OPND378	OPND379
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01A4 1800 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01A5 3000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01A6 9600 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01A7 4800 AC00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01A8 4800 2000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01A9 0200 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01AA 0500 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

ENDCHARSTRING: IF NOT LC2 THEN STEP ELSE SKIP
NEMCARD - 1 = MPCR
A1 = MIR
LIT = MAR2
NXTINSTR = LIT
OUT - 1 = MPCR

SWITCHES:
INPUT - 1 = CPCR
B R = A1
16 = SARI 63 = LIT
LIT AND B = A1
LIT AND B = A1
PSW = LIT
INPUT - 1 = CPCR
A1 EOL LIT
1 = LIT
IF TRUE THEN STEP ELSE SKIP
SETCOL30 - 1 = MPCR
B C = B, CSAP
29 = SARI 1 = LIT
LIT OR B = B
B C = B, MIR
OUT - 1 = MPCR
SETCOL30: B C = B, CSAR
30 = SARI 1 = LIT
LIT OR B = B
B C = MIR
OUT - 1 = MPCR

TRACE: LIT = MAR2, BEX
B R = B
B R = B
16 = SARI 63 = LIT
LIT AND B = A2
1 = SAR
A2 EOL 1
IF TRUE THEN B101 C = A1 SKIP
B100 = A1
INPUT - 1 = CPCR
A1 OR B = MIR
OUT - 1 = MPCR

01AB 0460 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01AC 0300 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01AE 4800 A150 AC00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01AF 4800 2000 CC00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B0 0460 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B2 4800 A150 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B3 0010 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B4 6800 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B5 0200 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B6 4800 0C41 8800 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B7 9010 0000 CC00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B8 4800 2C00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01B9 4800 0C41 8800 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01BA 0500 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01BB 4800 0C41 8800 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01BC 4010 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01BD 4800 2C00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01BE 4800 0C41 8800 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01BF 0500 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

01C0 4800 2000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C1 0200 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C2 0300 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C3 0300 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C4 4800 2C00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C5 1000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C6 4800 CC02 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C7 6C10 1801 CC00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C8 4800 1800 4000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01C9 0460 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01CA 4800 AC00 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
01CB 0500 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

06659000 0
06660000 0
06661000 0
06662000 0
06663000 0
06664000 0
06665000 0
06666000 0
06667000 0
06668000 0
06669000 0
06670000 0
06671000 0
06672000 0
06673000 0
06674000 0
06675000 0
06676000 0
06677000 0
06678000 0
06679000 0
06680000 0
06681000 0
06682000 0
06683000 0
06684000 0
06685000 0
06686000 0
06687000 0
06688000 0
06689000 0
06690000 0
06691000 0
06692000 0
06693000 0
06694000 0
06695000 0
06696000 0
06697000 0
06698000 0
06699000 0
06700000 0
06701000 0
06702000 0
06703000 0
06704000 0
06705000 0
06706000 0
06707000 0
06708000 0
06709000 0
06710000 0
06711000 0
06712000 0
06713000 0
06714000 0
06715000 0
06716000 0
06717000 0

% THIS ROUTINE WILL EMULATE THE PHYSICAL
% SETTING OF THE UYK-20 PROGRAM STOP
% SWITCHES 1 AND 2. HAR2 CONTAINS ADDR
% ADDRESS OF COL 1-9. COL 2 WILL CONTAIN 06700000
% A 1 INDICATES SWP1 ON OR A 2 INDICATES SWP2 ON
% SWP2 IS ON. BITS 30 AND 29 OF THE
% PSW WILL BE SET TO A 1 IF TO INDICATE
% SWITCH 1 AND SWITCH 2 RESPECTIVELY.
% RENEW COLS 1-4 INTO B
% COL 2 INTO LS BYTE OF A1
% MASK OUT LS BYTE OF A1
% HAR2 CONTAINS ADDR OF PSW
% CHECK IF SWP1 SET
% READ INTO B THE CONTENTS OF THE PSW
% SET COL 30
% SET COL 29 (OFF FAULTS TO SWP2 BEING SET)
% SET BIT 29
% RESTORE P
% SET BIT 30
% RESTORE F VALUE IN MIR
% THIS ROUTINE SETS THE 2 MS BITS IN SWP2 INTO
% SWP1 AND SWP2. COLS TO SET OR PIR
% ISOLATE COL 2 OF CONTROL CARD
% IF 1 THEN SET MS 2 BITS OF SWP2 (CRT)
% A2 CONTAINS COL 2 OF CONTROL CARD
% IS COL 2 A 1?
% ALL SKIP
% PRIMER MASK
% SWP2 INTO B
% SET MSB OF SW B 2
%
% AN/UYK-20 EMULATOR
%
% UTILITY ROUTINES
%
%

```



```

AED0:
THIS ROUTINE TESTS IF THE A1 FIELD
EQUALS THE A1 FIELD. IF EQUAL LC2
A2 = RMJ B = RA RETURNED
    IF LC2
    A3 R = B
    A = SARJ 15 = LIT
    LIT AND B = A2
    A3 AND LIT = A2
    A2 EOL B
    IF TRUE THEN SET LC2
    JUMP

BUMP:
A1 L = A2
COMP 164 SAR
A2 R = A2
A2 GTR 0 = A2
IF FALSE THEN A1 + 1 = MPGR
OPCODE - 1 = MPGR
A1 R = A1
15 = SAR
A1 L = A1
COMP 10 = SAR
A1 OR B = A1
OPCODE - 1 = MPGR

BYTETEST:
B
IF LST THEN SET LC2 SKIP IF LSB OF B EQUALS 1 THEN SET LC2
IF LC2
B R = B
1 = SAR
JUMP

***** CARRY BIT SETTING *****
CARRY:
IF LC1 THEN STEP ELSE SKIP THIS ROUTINE WILL SET THE CARRY
SETCARRY - 1 = MPGR
CLEARC - 1 = MPGR

CLEARC:
A1 C = A1
28 = SAR
A1 AND B110 = A1,CSAR
A1 C = A1
JUMP

SETCARRY: A1 C = A1

C1C0 3809 0000 0000 00F0
C1CD 4809 0000 8000 00F0
C1CE 50F0 00C3 0030 0080
C1CF 4809 2C56 0030 00FC
C1D0 4809 E156 2C00 00F0
C1D1 4809 CC52 0C30 00F0
C1D2 5449 0000 0000 00F0
C1D3 4820 00C0 0C30 00F0

C1D4 4809 A0C1 2030 00F0
C1D5 8000 00C0 0000 002C
C1D6 4809 C0B0 A0C0 00F0
C1D7 4809 C0B0 A0C0 00F0
C1D8 78C8 00C0 00C0 00F0
C1D9 78C8 00C0 00C0 00F0
C1DA 829C 0000 0C30 0080
C1DB 4809 A0B0 C030 00F0
C1DC 0C00 0000 0C30 0020
C1DD 4809 A0C1 4000 00F0
C1DE 4809 00C1 0030 00F0
C1DF 40C0 00C3 0C30 0020
C1E0 4809 AC53 4030 00F0
C1E1 02AC 00C0 0000 0040

C1E2 48D9 0C43 0070 00F0
C1E3 5A59 00D3 0070 00F0
C1E4 3809 00C3 0C30 00FC
C1E5 4809 0C40 8030 00F0
C1E6 1000 0000 0C30 0000
C1E7 4820 00C0 0C30 00F0

C1E8 280B 0000 0070 00F0
C1E9 0200 0000 0000 0040
C1EA 02C0 0000 0C30 004C

C1EB 4809 A0C1 C030 00FC
C1EC 8000 00C0 0C30 0030
C1ED 4809 A0CE 4000 40F0
C1EE 4809 ACCL C030 00F0
C1EF 4820 00C0 0030 00F0

C1F0 4809 A0C1 C030 00F0

```


[illegible]


```

0217 4809 46C1 8800 00F0
0218 000C 0000 0000 004C
0219 2809 0000 0000 00F0
021A 4809 AC5C 4030 00F0
021B 4820 0000 0030 00F0

SFT00:
021C 4809 1809 8870 00FC
021D 0000 0000 0C70 00F0
021E 4809 AC55 4030 00F0
021F 4820 0003 0C7C 00F0

SET01:
0220 4809 1800 880C 00F0
0221 000C 0000 0000 001C
0222 4809 AC5C 4030 00FC
0223 4809 1819 880C 00FC
0224 3C00 0C00 003C 0000
0225 4809 AC55 4030 00FC
0226 4820 0019 0070 00F0

CHECK0C:
0227 4809 A0C1 C020 40F0
0228 3030 0003 007C 0040
0229 4809 A156 0B7C 00FC
022A 4809 A001 C070 00FC
022B 4820 0003 0000 00F0

***** END CONDITION CODE ROUTINES *****
CONTENTSRA:
AMPCR = A2
B R = B
4 = SAR; 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
ASE = B
BMR = B
COMP - 16 = SAR
B OR A3 = A3
EINPUL - 1 = CPCR
A2 = AMPCR
JUMP

CONTENTSRRH:
AMPCR = A2
A3 AND LIT = B
15 = LIT

022C 4809 0640 200C 00F0
022D 4809 0C40 883C 00F0
022E 40F0 0000 000C 0080
022F 4809 2C56 0B3C 00FC
0230 0370 000C 0C0C 0060
0231 4809 0C40 883C 24FC
0232 4809 0C40 883C 00F0
0233 4809 0000 0C00 0020
0234 000C 0000 0C00 0020
0235 4809 EC5C 4030 00FC
0236 0380 0003 000C 0060
0237 4809 0C00 0C1C 00F0
0238 4820 6C00 0070 00F0

0239 4809 0640 2C70 00FC
023A 4809 E156 0B7C 00F0
023B 00FC 000C 0070 0060

```



```

0245 9809 C138 0030 00FC 01045000 0
0246 909C 0000 0030 00E0 01045000 0
0247 7C0B C140 2C30 00F0 01027C00 0
0248 0076 0000 00C0 00E0 01027C00 0
0249 9809 C041 8030 00F0 01022600 0
0250 0000 0000 0030 0010 01023C30 0
0251 9809 0C40 0030 00F0 01024400 0
0252 9809 0B02 8B32 00F0 01025400 0
0253 0040 0000 0030 00B0 01026C00 0
0254 9809 A003 001C 00F0 01027600 0
0255 9809 2C52 0C30 00F0 01028C00 0
0256 680C 00C3 0030 00E0 01029C00 0
0257 0460 0000 0030 0060 01030C00 0
0258 2F59 A0C0 4C30 00F0 01031C00 0
0259 2F59 0000 0030 00F0 01032C00 0
0260 2A0B 0000 0030 00F0 01033C00 0
0261 241C 0000 0030 004C 01034C00 0
0262 9809 0000 0030 00F0 01035C00 0
0263 800C 0000 00B0 00F0 01036C00 0
0264 241C C0F0 0000 0040 01037C00 0
0265 9809 0000 001C 00F0 01038C00 0
0266 9809 0000 0030 0060 01040C00 0
0267 9809 0F40 9000 00F0 01042C00 0
0268 000C 0000 0030 0010 01043C00 0
0269 9809 E0C3 1030 00F0 01044C00 0
0270 9809 E132 0030 00F0 01045C00 0
0271 680C E132 0C30 00F0 01047C00 0
0272 0480 0000 0030 0060 01048C00 0
0273 01FC 0000 0030 00F0 01050C00 0
0274 01FC 0000 0030 00F0 01051C00 0
0275 0490 0000 0030 0060 01052C00 0
0276 0180 0000 0030 0060 01053C00 0
0277 680C E132 0C00 00FC 01054C00 0
0278 0440 0000 0030 0060 01055C00 0
0279 020C 0000 0030 00E0 01057C00 0
0280 680C E132 0000 00F0 01058C00 0
0281 040C 0000 0030 0060 01059C00 0
0282 060C E132 0030 00FC 01061C00 0
0283 9809 E0C3 0030 00F0 01062C00 0
0284 280B C000 0030 0040 01064C00 0
0285 297C C000 0030 0040 01065C00 0
0286 9809 A180 403C 00F0 01067C00 0
0287 0020 0000 0030 00E0 01068C00 0
0288 9809 E138 0C30 00F0 01070C00 0
0289 02FA 0000 0030 00F0 01071C00 0
0290 798C 0000 0030 0040 01072C00 0
0291 1F4C 0000 0030 0060 01073C00 0
0292 04FC 0000 0030 0060 01074C00 0
0293 0540 0000 0030 0060 01075C00 0
0294 9809 20C3 001C 00F0 01076C00 0
0295 0260 0000 0030 00E0 01077C00 0

```



```

0306 4809 0640 0C40 00F0
0307 4809 20C3 001C 00F0
0308 02C0 00C3 0C40 00F0
0309 2F5C 00C0 0C40 00C0
030A 4809 0000 0000 20F0
030B 4809 0F43 001C 00F0
030C 4809 0000 9000 00F0
030D 0000 00C3 0000 00C0
030E 4809 00C1 1000 00F0
030F 05AC 0000 0000 00C0
0310 4809 0C41 2050 00F0
0311 0000 0000 0000 00F0
0312 4809 0F43 001C 00F0
0313 0500 0000 0000 00C0
0314 0500 0000 0000 00C0
0315 4809 0C40 0000 00F0
0316 4809 0F46 0B30 00F0
0317 4809 0000 0000 20F0
0318 4809 0F43 801C 00F0
0319 0000 00C0 0000 001C
031A 4809 0C41 0020 00F0
031B 4809 0000 0000 24F0
031C 4809 0F41 001C 00F0
031D 05C0 0C43 0C00 00C0
031E 4809 0F40 2000 00F0
0320 032C 0003 0C00 00F0
0321 4809 20C3 001C 00F0
0322 2F30 0003 0C00 00C0
0323 4809 0000 0000 20F0
0324 4809 0F43 0C10 00F0
0325 4809 0C41 0020 00F0
0326 0000 00C0 0000 0030
0327 4809 0000 0C00 00F0
0328 4809 0000 0000 00F0
0329 021C 0003 0050 00F0
032A 4809 0C40 4030 00F0
032B 3E53 0C42 0000 00F0
032C 4809 0C43 0020 00F0
032D 5819 0000 0000 00F0
032E 30E0 0000 0000 0000
032F 4809 20C3 001C 00F0
0330 02C0 0003 0000 00F0
0331 2F3C 00C3 0C00 00C0
0332 4809 0C40 0040 00F0
0333 4809 0000 0000 00F0
0334 4820 00C0 0030 00F0

```

```

COMPRESS:
% INPUT OUTPUT CONTROL
% THIS ROUTINE COMPRESSES JNUTK00
% 16 BIT BUFFERS (LHW 16 32 BIT) OVERGROWS
% 5-HEBRY WORD INTO A 32 BIT WORD
% FORMAT COMPATIBLE WITH THE IOP
% UPON ENTRY, B1 CONTAINS BUFFER ADDRESS 01149000
% N04 OF BUFFERS IN UHW OF A3
% THIS ROUTINE ACCEPTS A VARIABLE
% BUFFER LENGTH FOR CRT OUTPUT, J3 WORUS
% FOR FRT OUTPUT
% STORE AMPCR INTO STACK
% (STACK) = AMPCR
% REFERENCE B1
% STORE BUFFER ADDRESS IN ER2
% CLEAR LHW OF A3 FOR COUNT
% GET CONTENTS OF BUFFER ADDRESS WORD
% STORE CONTENTS IN UHW OF A2
% GET ADJACENT WORD ADDR.
% B = CONTENTS OF ADJACENT WORD
% COMPLEMENT TO NEXT 32 BIT WORD
% STORE NEXT WORD PAIR ADDR. IN B
% REFERENCE B1
% COMPRESSED WORD DESTINATION
% STORE WORD PAIR ADDR. IN B
% REFERENCE BR2
% COMPRESSED WORD DESTINATION IN BR2
% SAVE DESTINATION ADDR. IN B
% BUFFER LENGTH IN 10CW + 2
% 10CW + 2 = HAR2
% B = BUFFER LENGTH
% REFERENCE BR1
% TRANSFER NEXT WORD PAIR ADDR TO BR2
% NEXT DESTINATION ADDR. IN BR1
% INCREMENT COUNTER ( < 2 16 - 1 )
% ISOLATE COUNTER IN A2
% LIT
% RESTORE AMPCR FROM STACK
% SEPARATE AMPCR ASSIGNMENTS AND JUMP
%
%
%

```



```

0335 4809 0000 0070 20F0
0336 4809 CF40 A030 00F0
0337 0000 0000 0030 00F0
0338 4809 E0C1 0070 00F0
0339 0000 0000 0030 0020
033A 4809 0040 8B3F 00F0
033B 4809 C040 7000 00F0
033C 4809 C00E 2000 00F0
033D 4809 0641 0020 00F0
033E 0000 0000 0030 0030
033F 4809 C001 0010 00F0
0340 0000 0000 0030 0060
0341 0000 0000 0030 0020
0342 0000 0000 0030 0020
0343 4809 C003 8030 00F0
0344 4809 E001 2070 00F0
0345 4809 C000 0030 00F0
0346 4809 CF41 0010 00F0
0347 0000 0000 0030 0030
0348 0500 0000 0000 0060
0349 4809 0F40 2070 00F0
034A 4809 E0C1 0800 00F0
034B 0000 0000 0030 0020
034C 4809 C000 0030 00F0
034D 4809 C000 880F 00F0
034E 4809 C00F 0010 00F0
034F 0000 0000 0030 0030
0350 05F0 0000 0030 0060
0351 4809 0040 8C30 00F0
0352 0000 0000 0070 0020
0353 4809 E00F 2030 00F0
0354 4809 C000 AC30 00F0
0355 4809 CF41 0010 00F0
0356 0000 0000 0030 0030
0357 0500 0000 0000 0060
0358 4809 E00E 2030 00F0
0359 4809 E00E 2030 00F0
035A 0000 0000 0030 0020
035B 4809 C003 4800 00F0
035C 4809 C012 0000 00F0
035D 5010 0000 0030 00F0
035E 0610 0000 0020 0040
035F 4805 0F40 2000 00F0
0360 4809 C000 0030 00F0
0361 0000 0000 0030 0030
0362 33F0 0000 0000 0040
0363 4809 C000 0030 20F0
0364 4809 0F40 8040 00F0
0365 0000 0000 0030 0010
0366 4809 0000 0070 00F0
0367 4820 C003 0000 00F0

```

ASR
 DMAR R = A2
 B = SAR
 A3 L = B
 COMP 16 = SAR
 D R = B
 A2 + B = A2
 A2 - 1 = A2
 AMPCR L = BR1
 COMP 8 = SAR
 A2 L = BR2
 ENULIN - 1 = CPCR
 ENULIN - 1 = A2
 COMP 16 = SAR
 A2 R = MIPR ASE
 A3 L = A2
 A2 R = A2
 A2 + BHAR L = BR2
 COMP 8 = SAR
 ENULOUT - 1 = CPCR
 ASE
 BHAR = A2
 A3 L = D
 COMP 16 = SAR
 B R = D
 A2 - B L = BR2
 COMP 8 = SAR
 ENULIN - 1 = CPCR
 B R = MIP
 16 = SAR
 A2 R = A2
 A2 + BHAR L = BR2
 COMP 8 = SAR
 ENULOUT - 1 = CPCR
 A3 - 1 L = A2
 16 = SAR
 A2 + BHAR L = BR2
 COMP 8 = SAR
 ENULOUT - 1 = CPCR
 A3 - 1 L = A2
 COMP 16 SAR
 A2 R = A2, B
 A2 EOL 0
 IF FALSE THEN SKIP
 EXPEND - 1 = MPCR
 BHAR = A2
 A2 - B - 1 L = DR2
 COMP 8 = SAR
 EXPRT - 1 = MPCR
 ASR
 RHAR R = AMPCR
 B = SAR
 STEP
 JUMP

EXPANDIT
 THIS ROUTINE WILL TAKE A ROUTINE
 CONTAINING 32 BIT WORDS AND EXPAND EACH
 INTO 2 - 32 BIT WORDS, PUTTING THE
 IN THE LOW OF EACH 32 BIT WORD.
 BR1 MUST CONTAIN THE BUFFER ADDRESS
 AND A3 MUST CONTAIN # OF BUFFERS/COUNT
 REFERENCE BR1
 ISOLATE THE COUNT(BUFFER EXPAND FACTOR)
 CALCULATE FIRST OUTPUT ADDRESS
 RETURN IN BR1
 BUFFER ADDR + BEF - 1 IN BR2
 CONTENTS OF 1 WORD INTO C
 WORD CONTENTS INTO UNM OF A2
 ISOLATE BUFFER COUNT
 BUFFER ADDR + COUNT INTO BR2
 OUTPUT 1 EXPANDED HALFWORD
 REFERENCE MAR2
 ISOLATE THE COUNT
 COUNT INTO B
 NEXT READ ADDRESS INTO BR2
 NEXT WORD INTO B
 REDUCE THE COUNT BY 1
 NEXT WRITE ADDRESS
 WRITE OUT NEXT EXPANDED WORD
 REDUCE THE COUNT
 CHECK IF ALL WORDS EXPANDED
 NEXT READ ADDRESS
 REFERENCE BR1
 RESTORE RETURN ADDRESS
 REFERENCE BR1
 THIS ROUTINE DUMPS THE BUFFERS

EOUT:

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0320 2630 00C0 00D0 00E0 00F0
032E 4809 0C40 0030 00F0
033F 4809 00C1 0F30 00F0
0340 0C00 00C0 00C0 00F0
0341 4809 0C40 0030 00F0
0342 0680 00C0 00C0 00F0
0343 39AC 00C0 00D0 0040
0344 4809 E0C0 A0C0 00FC
0345 00C0 C0D0 00C0 00C0
0346 4809 E0C0 20C0 00F0
0347 4809 E0C1 90C0 00F0
0348 4809 E0D0 10C0 00F0
0349 48C9 1FC1 90D0 00FC
03AA 48C9 C012 00C0 00FC
03AB 6019 00C0 00C0 00F0
03AC 0690 00C0 00C0 0040
03AD 4809 20C3 001C 00F0
03AE 0320 00D0 00C0 00E0
03AF 253C 00C0 00C0 0060
03B0 0809 2C41 0020 00F0
03B1 4809 00C0 00C0 00F0
03B2 4809 2C40 0030 00F0
03B3 2F50 00C0 C0C0 0060
03B4 3990 00C3 00D0 C040

IN:
03B5 3809 C0C0 00C0 C0F0
03B6 4809 C0C3 A0C0 00F0
03B7 A0D0 00C0 00C0 0010
03B8 48C9 C640 00C0 00F0
03B9 06A0 00C0 0C30 00C0
03BA 48C9 00C0 00C0 00F0
03BB 4824 00C3 00C0 00F0

INDEV:
03BC 0680 00C3 00D0 0040
03BD 06CC 00D0 90D0 0040
03BE 06C0 00C3 00D0 0040

SP01:
03BF 4809 20C3 001C 00F0
03C0 032C 00D0 00C0 00EC
03C1 4809 00C0 00C0 0060
03C2 4809 0C40 0030 00F0
03C3 4809 0C41 002C 00F0
03C4 08C0 00C3 00C0 0030
03C5 48C9 20C1 00C0 00F0
03C6 0060 00C0 00D0 C040
03C7 48C9 0C40 0030 00F0
03C8 06E0 00C3 00C0 0040
03C9 38E0 00C0 00C0 00C0
03CA 48C9 E0C0 90D0 00FC
03CB 00C0 00C0 00C0 0020
03CC 4809 E0C1 1C00 00F0
03CD 4809 E0C1 1000 00F0
03CE 4809 E1C3 1000 00F0
03CF 014C 00C0 00C0 00E0
03D0 334C 00C0 00C0 0060
03D1 4809 E0C3 40D0 00FC

% STORE BUFFER ADDRESS IN IIR
% IS COUNTER = 0
% REGENERATE BUFFER ADDRESS
% WRITE NEW ADDRESS IN BR1
% WRITE NEW BUFFER ADDR IN I0C4 + 1
% THIS ROUTINE INPUTS DATA FROM
% PERIPHERAL DEVICES TO THE DESIGNATED
% BUFFERS. CRO READER, CRT, OR DISK (N1)
% CLEAR LC2
% A2 = (I0C4)
% A2 CONTAINS DEVICE CODE
%
% DISK NOT IMPLEMENTED
% READ SP0 FUNCTION:
% RETRIEVE BUFFER ADDR.
% STORE BUFFER ADDR IN M1R
% STORE ADDRESS IN BR1
% ISOLATE COUNTER
% DECREMENT COUNTER
% RESTORE A3, LHM CLEARED
% BUFFER EXPANSION FACTOR IN LHM OF A3
% EXPAND BUFFER
% ISOLATE COUNTER

```



```

C402 4809 2003 001C 00F0
C403 02CC 0000 0000 00E0
C404 4809 E000 0000 00F0
C405 2F5C 0003 0000 00E0
C406 0720 0003 00C0 00E0
C407 0000 0000 0000 00E0
C408 0000 0000 0000 00E0
C409 4809 0000 9C00 00F0
C40A 4809 0041 0020 00F0
C40B 4809 LC5C 1000 00F0
C40C 230C 0003 0070 00E0
C40D 4809 E000 AC00 00F0
C40E 0000 0000 0070 00E0
C40F 4809 CC00 0030 00F0
C410 0730 0000 0070 00E0

C411 4809 2003 001C 00F0
C412 02CC 0003 0030 00E0
C413 4809 E000 0030 00E0
C414 2F5C 0000 00C0 00E0
C415 074C 0003 0000 00E0
C416 0750 0000 00C0 00E0

C417 4809 E001 1070 00F0
C418 0000 0000 00C0 00E0
C419 4809 E003 3070 00F0
C41A 4809 0041 0010 00F0
C41B 0000 00C0 0000 003C
C41C 4809 0041 003C 00F0
C41D 0000 0000 0000 0020
C41E 4809 EC5C 1070 00F0
C41F 076C 0000 0070 00E0
C420 4809 CC40 AC00 00F0
C421 400C 0000 0030 0010
C422 4809 C0C3 C070 00F0
C423 5600 0000 0000 00F0
C424 077C 0000 C000 00C0
C425 0780 0000 0000 00E0

C426 4809 18C1 AC0C 00E0
C427 3000 00C3 0030 00E0
C428 4809 CC5C AC00 00F0
C429 300C 0000 0070 001C

I1W1 AT Y = IY1 + (RCH)
% LC2 INDICATES BYTE INSTRUCTION
% ROUTINES RETURN B = Y

% STORE A3 WITH RETURN ADDR. IN STACK
% WRITE TO EMULATION RESERVE BUFFER
% CLEAR UHW OF A3
% UHW OF A3 CONTAINS IY1
% LHW OF A3 CONTAINS INSTRUCTION
% B = (RCH)
% A2 CONTAINS IY1
% CALCULATE ADDRESS OF Y
%
% INDIRECT ADDRESSING WITHOUT INDEXING
% IY AT Y = IY1
% LC2 INDICATES BYTE INST. ROUTINE
% RETURNS B = Y AND A2 = (RCH)
% WRITE A3 WITH RETURN IN UHW
% RETRIEVE IY1 FIELD
%
% THIS ROUTINE READS IN IY1 AND TESTS
% IF CASCADED OR DIRECT ADDRESSING IS
% REQUIRED.
% CLEAR UHW OF A3
%
% U2 = IY1 ADDRESS
% SAVE IY1 ADDR IN UHW OF A3
% B = (IY1)
% TEST IF BIT 14 OF IY1 IS SET
% IF BIT SET, CASCADED IY
% IF BIT NOT SET, FORM Y
%
% THIS ROUTINE DECIDES WHICH ADDRESSING
% FORMULA TO USE TO COMPUTE THE NEW
% LOCATION OF THE INDIRECT WORD
% A2 IS BIT MASK FOR J FIELD OF IY
%
I1W1 AT Y = IY1 + (RCH)
% LC2 INDICATES BYTE INSTRUCTION
% ROUTINES RETURN B = Y

% STORE A3 WITH RETURN ADDR. IN STACK
% WRITE TO EMULATION RESERVE BUFFER
% CLEAR UHW OF A3
% UHW OF A3 CONTAINS IY1
% LHW OF A3 CONTAINS INSTRUCTION
% B = (RCH)
% A2 CONTAINS IY1
% CALCULATE ADDRESS OF Y
%
% INDIRECT ADDRESSING WITHOUT INDEXING
% IY AT Y = IY1
% LC2 INDICATES BYTE INST. ROUTINE
% RETURNS B = Y AND A2 = (RCH)
% WRITE A3 WITH RETURN IN UHW
% RETRIEVE IY1 FIELD
%
% THIS ROUTINE READS IN IY1 AND TESTS
% IF CASCADED OR DIRECT ADDRESSING IS
% REQUIRED.
% CLEAR UHW OF A3
%
% U2 = IY1 ADDRESS
% SAVE IY1 ADDR IN UHW OF A3
% B = (IY1)
% TEST IF BIT 14 OF IY1 IS SET
% IF BIT SET, CASCADED IY
% IF BIT NOT SET, FORM Y
%
% THIS ROUTINE DECIDES WHICH ADDRESSING
% FORMULA TO USE TO COMPUTE THE NEW
% LOCATION OF THE INDIRECT WORD
% A2 IS BIT MASK FOR J FIELD OF IY
%

```


042A	4809	C640	0030	00F0	A2 + AMPCR = AMPCR	% COMPUTE FORMULA DESIRED	0148F000 D
042B	079C	0003	0030	C0C0	INADDR - 1 = AMPCR		01499F00 D
042C	4809	0000	0030	00F0	STEP		01500400 D
042D	4824	0000	0030	00F0	EXEC		01502000 D
042E	07A0	0000	0030	0040			01503100 D
042F	07A0	0000	0030	0040	AD10 - 1 = MPCR		01504000 D
0430	07A0	0000	0030	0040	AD11 - 1 = MPCR		01505100 D
0431	07A0	0000	0030	0040	AD12 - 1 = MPCR		01506100 D
0432	07A0	0000	0030	0040	AD13 - 1 = MPCR		01507000 D
0433	4809	E0D0	A030	00F0			01508F00 D
0434	000C	0000	0030	0020	A3 R = A2	% NEW 1W AT Y = 1W2	01509F00 D
0435	000C	0003	0030	00F0	16 = SAR	% SHIFT ADDR OF 1W INTO A2	01510C00 D
0436	070C	0000	0030	003C	A2 OR 1 L = BR2	% NEXT ADDRESS OF 1W	01512C00 D
0437	070C	0000	0030	003C	COMP 8 = SAR		01513C00 D
0438	000C	0000	0030	003C	ENULIN - 1 = CPCR	% R CONTAINS 1W2; Y = 1W2	01514C00 D
0439	416C	00C0	0030	0040	INDIRMO - 1 = MPCR	% Y = NEXT ADDR OF 1W1	01515C00 D
043A	000C	0000	0030	003C			01516C00 D
043B	000C	0000	0030	003C			01517C00 D
043C	000C	0000	0030	003C			01518000 D
043D	000C	0000	0030	003C			01518000 D
043E	000C	0000	0030	003C			01519C00 D
043F	000C	0000	0030	003C			01520C00 D
0440	000C	0000	0030	003C			01521C00 D
0441	000C	0000	0030	003C			01522C00 D
0442	000C	0000	0030	003C			01523C00 D
0443	000C	0000	0030	003C			01524C00 D
0444	000C	0000	0030	003C			01525C00 D
0445	000C	0000	0030	003C			01526C00 D
0446	000C	0000	0030	003C			01527C00 D
0447	000C	0000	0030	003C			01528C00 D
0448	000C	0000	0030	003C			01529C00 D
0449	000C	0000	0030	003C			01530C00 D
044A	000C	0000	0030	003C			01531C00 D
044B	000C	0000	0030	003C			01532C00 D
044C	000C	0000	0030	003C			01533C00 D
044D	000C	0000	0030	003C			01534C00 D
044E	000C	0000	0030	003C			01535C00 D
044F	000C	0000	0030	003C			01536C00 D
0450	000C	0000	0030	003C			01537C00 D
0451	000C	0000	0030	003C			01538C00 D
0452	000C	0000	0030	003C			01539C00 D
0453	000C	0000	0030	003C			01540C00 D
0454	000C	0000	0030	003C			01541C00 D
0455	000C	0000	0030	003C			01542C00 D
0456	000C	0000	0030	003C			01543C00 D
0457	000C	0000	0030	003C			01544C00 D
0458	000C	0000	0030	003C			01545C00 D
0459	000C	0000	0030	003C			01546C00 D
045A	000C	0000	0030	003C			01547C00 D
045B	000C	0000	0030	003C			01548C00 D
045C	000C	0000	0030	003C			01549C00 D
045D	000C	0000	0030	003C			01550C00 D
045E	000C	0000	0030	003C			01551C00 D
045F	000C	0000	0030	003C			01552C00 D
0460	000C	0000	0030	003C			01553C00 D
0461	000C	0000	0030	003C			01554C00 D
0462	000C	0000	0030	003C			01555C00 D
0463	000C	0000	0030	003C			01556C00 D
0464	000C	0000	0030	003C			01557C00 D


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0044E 3000 0000 0000 0020      A9 = SAR
0045E 4809 C0C3 00C0 0040      A2 AND B R = A2
0046E 4809 C0C3 00C0 0040      12 = SAR
0047E 3000 0000 0000 0010      A2 = SAR
0048E 3000 0000 0000 0010      12 = SAR
0049E 4809 C640 00C0 00F0      A2 + AMPCR = AMPCR
004AE 4809 C640 00C0 00F0      DTRADDR - 1 = AMPCR
004BE 085C 0000 0000 005E      STEP
004CE 4809 0000 0000 00F0      EXEC
004DE 4824 0000 00C0 00F0      EXEC

DIRADDR: 010 - 1 = MPCR
          011 - 1 = MPCR
          012 - 1 = MPCR
          013 - 1 = MPCR

DT0:     A3 R = A2
          16 = SAR
          A2 OR 1 L = BR2
          COMP 8 = SAR
          EMULTN - 1 = CPGR
          IF LC2
          DTRETURN - 1 = MPCR

          B AND LIT = B
          15 = LIT
          REGSTACK - 1 = CPGR
          FINPUT - 1 = CPGR
          DTGN - 1 = MPCR

DT1:     A3 AND LIT = B
          15 = LIT
          REGSTACK - 1 = CPGR
          FINPUT - 1 = CPGR
          DTGN - 1 = MPCR

DT2:     A3 AND LIT = B
          15 = LIT
          REGSTACK - 1 = CPGR
          FINPUT - 1 = CPGR
          DTGN - 1 = MPCR

DT3:     A3 AND LIT = B
          15 = LIT
          REGSTACK - 1 = CPGR
          FINPUT - 1 = CPGR
          DTGN - 1 = MPCR

DTGN:     THIS ROUTINE COMPUTES Y, TEST FOR BYTE
           INST., AND RETURN TO CALLER OF
           RXFIELD
           IW1 ADDR INTO BR2 INC. BY 1
           16 = SAR
           A2 OR 1 L = PR2
           COMP 8 = SAR
           P = A2
           EMULTN - 1 = CPGR
           A2 = NIR
           4809 E0C3 AC0C C0F0
           4871 0000 00C3 00C0 C020
           4872 4809 C0C3 0010 CFCF
           4873 0000 00C3 000C 003C
           4874 4809 C0C0 20C0 00F0
           4875 092C 00C3 00C0 006C
           4876 4809 C0C3 003C 00F0
           4877 0000 00C3 000C 00F0
           4878 4809 C0C3 000C 00F0
           4879 0000 00C3 000C 00F0
           4880 0000 00C3 000C 00F0
           4881 0000 00C3 000C 00F0
           4882 0000 00C3 000C 00F0
           4883 0000 00C3 000C 00F0
           4884 0000 00C3 000C 00F0
           4885 0000 00C3 000C 00F0
           4886 0000 00C3 000C 00F0
           4887 0000 00C3 000C 00F0
           4888 0000 00C3 000C 00F0
           4889 0000 00C3 000C 00F0
           4890 0000 00C3 000C 00F0
           4891 0000 00C3 000C 00F0
           4892 0000 00C3 000C 00F0
           4893 0000 00C3 000C 00F0
           4894 0000 00C3 000C 00F0
           4895 0000 00C3 000C 00F0
           4896 0000 00C3 000C 00F0
           4897 0000 00C3 000C 00F0
           4898 0000 00C3 000C 00F0
           4899 0000 00C3 000C 00F0
           4900 0000 00C3 000C 00F0
           4901 0000 00C3 000C 00F0
           4902 0000 00C3 000C 00F0
           4903 0000 00C3 000C 00F0
           4904 0000 00C3 000C 00F0
           4905 0000 00C3 000C 00F0
           4906 0000 00C3 000C 00F0
           4907 0000 00C3 000C 00F0
           4908 0000 00C3 000C 00F0
           4909 0000 00C3 000C 00F0
           4910 0000 00C3 000C 00F0
           4911 0000 00C3 000C 00F0
           4912 0000 00C3 000C 00F0
           4913 0000 00C3 000C 00F0
           4914 0000 00C3 000C 00F0
           4915 0000 00C3 000C 00F0
           4916 0000 00C3 000C 00F0
           4917 0000 00C3 000C 00F0
           4918 0000 00C3 000C 00F0
           4919 0000 00C3 000C 00F0
           4920 0000 00C3 000C 00F0
           4921 0000 00C3 000C 00F0
           4922 0000 00C3 000C 00F0
           4923 0000 00C3 000C 00F0
           4924 0000 00C3 000C 00F0
           4925 0000 00C3 000C 00F0
           4926 0000 00C3 000C 00F0
           4927 0000 00C3 000C 00F0
           4928 0000 00C3 000C 00F0
           4929 0000 00C3 000C 00F0
           4930 0000 00C3 000C 00F0
           4931 0000 00C3 000C 00F0
           4932 0000 00C3 000C 00F0
           4933 0000 00C3 000C 00F0
           4934 0000 00C3 000C 00F0
           4935 0000 00C3 000C 00F0
           4936 0000 00C3 000C 00F0
           4937 0000 00C3 000C 00F0
           4938 0000 00C3 000C 00F0
           4939 0000 00C3 000C 00F0
           4940 0000 00C3 000C 00F0
           4941 0000 00C3 000C 00F0
           4942 0000 00C3 000C 00F0
           4943 0000 00C3 000C 00F0
           4944 0000 00C3 000C 00F0
           4945 0000 00C3 000C 00F0
           4946 0000 00C3 000C 00F0
           4947 0000 00C3 000C 00F0
           4948 0000 00C3 000C 00F0
           4949 0000 00C3 000C 00F0
           4950 0000 00C3 000C 00F0
           4951 0000 00C3 000C 00F0
           4952 0000 00C3 000C 00F0
           4953 0000 00C3 000C 00F0
           4954 0000 00C3 000C 00F0
           4955 0000 00C3 000C 00F0
           4956 0000 00C3 000C 00F0
           4957 0000 00C3 000C 00F0
           4958 0000 00C3 000C 00F0
           4959 0000 00C3 000C 00F0
           4960 0000 00C3 000C 00F0
           4961 0000 00C3 000C 00F0
           4962 0000 00C3 000C 00F0
           4963 0000 00C3 000C 00F0
           4964 0000 00C3 000C 00F0
           4965 0000 00C3 000C 00F0
           4966 0000 00C3 000C 00F0
           4967 0000 00C3 000C 00F0
           4968 0000 00C3 000C 00F0
           4969 0000 00C3 000C 00F0
           4970 0000 00C3 000C 00F0
           4971 0000 00C3 000C 00F0
           4972 0000 00C3 000C 00F0
           4973 0000 00C3 000C 00F0
           4974 0000 00C3 000C 00F0
           4975 0000 00C3 000C 00F0
           4976 0000 00C3 000C 00F0
           4977 0000 00C3 000C 00F0
           4978 0000 00C3 000C 00F0
           4979 0000 00C3 000C 00F0
           4980 0000 00C3 000C 00F0
           4981 0000 00C3 000C 00F0
           4982 0000 00C3 000C 00F0
           4983 0000 00C3 000C 00F0
           4984 0000 00C3 000C 00F0
           4985 0000 00C3 000C 00F0
           4986 0000 00C3 000C 00F0
           4987 0000 00C3 000C 00F0
           4988 0000 00C3 000C 00F0
           4989 0000 00C3 000C 00F0
           4990 0000 00C3 000C 00F0
           4991 0000 00C3 000C 00F0
           4992 0000 00C3 000C 00F0
           4993 0000 00C3 000C 00F0
           4994 0000 00C3 000C 00F0
           4995 0000 00C3 000C 00F0

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00A3	4809	C640	2000	00F0	ASR	AMP CR = A2	% PAGE ADDRESSING IS ALLOWED	01679C00
00A4	4809	0000	0000	20F0	ASR	% SAVE RETURN IN A2	01679C00	
00A5	4809	0F43	0010	00F0	BHAR = DR2	% BR1 = BR2	01681000	
00A6	0970	0000	0000	00F0	EMULIN - 1 = CPCR	% G = (BR1)	01681000	
00A7	4809	0C40	0C30	00F0	R = MIR	% TRANSFER B TO MIR	01682C00	
00A8	4809	0C00	0000	00F0	A2 = B	% STORE AMP CR IN B	01683C00	
00A9	4809	E001	0C10	00F0	A3 L = BR2	% LHM OF A3 INTO BR2	01684C00	
00AA	0C00	0000	0000	00F0	COMP B = SAR	% LHM OF A3 INTO BR2	01685C00	
00AB	4809	E000	9C00	00F0	A3 R = A3	% ZERO OUT LHM OF A3	01686C00	
00AC	0000	0000	0000	00F0	16 = SAR	% ZERO OUT LHM OF A3	01687C00	
00AD	4809	E001	1C00	00F0	A3 L = A3	% STORE AMP CR IN LHM OF A3	01688C00	
00AE	4809	E5C0	1000	00F0	A3 OR B = A3	% STORE AMP CR IN LHM OF A3	01689C00	
00AF	0980	0000	9000	00F0	EMULOUT - 1 = CPCR	% STORE AMP CR IN LHM OF A3	01690C00	
00B0	4809	E001	2000	00F0	A3 L = A2	% STORE AMP CR IN LHM OF A2	01691C00	
00B1	0000	0000	0000	00F0	COMP 16 = SAR	% RETURN AMP CR TO LHM OF A2	01692C00	
00B2	4809	C000	AC00	00F0	A2 R = A2	% ZERO LHM OF A3	01693C00	
00B3	4809	E000	9000	00F0	A3 R = A3	% RETURN AMP CR TO LHM OF A2	01694C00	
00B4	4809	E001	1000	00F0	A3 L = A3	% ZERO LHM OF A3	01695C00	
00B5	4809	E5C0	1000	00F0	BHAR = B	% INCREMENT ADDRESS DESTINATION	01696C00	
00B6	4809	E5C0	1000	00F0	BHAR = A3, ASR	% STORE DESTINATION ADDR IN LHM OF A3	01697C00	
00B7	4809	0C40	8000	00F0	BHAR = B, CEAR	% INCREMENT ORIGIN	01698C00	
00B8	0000	0000	0000	00F0	B = SAR	% INCREMENT ORIGIN	01699C00	
00B9	4809	0C40	0000	00F0	B + 1 L = PR1	% SHIFT COUNT TO LHM OF A3	01700C00	
00BA	4809	E001	9C00	00F0	A3 C = A3	% DECREMENT COUNTER	01701C00	
00BB	0000	0000	0000	00F0	16 = SAR	% ISOLATE COUNTER IN LHM OF B	01702C00	
00BC	4809	E000	0000	00F0	A3 - 1 = A3, B	% RESTORE A3	01703C00	
00BD	4809	E001	0000	00F0	B L = B	% RESTORE A3	01704C00	
00BE	4809	0C40	8000	00F0	E R = B	% RESTORE A3	01705C00	
00BF	4809	E001	9000	00F0	A3 C = A3	% RESTORE A3	01706C00	
00C0	4809	0C52	0C30	00F0	R EOL 0	% RESTORE A3	01707C00	
00C1	0000	0000	0000	00F0	COMP B = SAR	% RESTORE A3	01708C00	
00C2	6000	0000	0000	00F0	IF FALSE THEN STEP ELSE SKIP	% RESTORE A3	01709C00	
00C3	4A3C	0000	0000	00F0	MRPT - 1 = MPCR	% RESTORE A3	01710C00	
00C4	4809	C000	0000	00F0	A2 = AMP CR	% RESTORE A3	01711C00	
00C5	48C9	C000	0000	00F0	STEP	% RESTORE A3	01712C00	
00C6	48C0	0000	0000	00F0	JUMP	% RESTORE A3	01713C00	
00C7	4809	0000	1000	00F0		% RESTORE A3	01714C00	
00C8	4809	0000	0000	00F0		% RESTORE A3	01715C00	
00C9	2009	0000	0000	00F0		% RESTORE A3	01716C00	
00CA	0990	0000	0000	00F0		% RESTORE A3	01717C00	
00CB	4809	0C52	0C30	00F0		% RESTORE A3	01718C00	
00CC	5400	C040	0000	00F0		% RESTORE A3	01719C00	
00CD	4409	C040	0000	00F0		% RESTORE A3	01720C00	
00CE	4C0B	C0C2	2000	00F0		% RESTORE A3	01721C00	
00CF	48C9	C000	2000	00F0		% RESTORE A3	01722C00	
00D0	4809	0C40	0C70	00F0		% RESTORE A3	01723C00	
00D1	4809	0C52	0B30	00F0		% RESTORE A3	01724C00	
00D2	2B19	C7C3	0000	00F0		% RESTORE A3	01725C00	
00D3	09AC	0000	0000	00F0		% RESTORE A3	01726C00	
00D4	48C9	C0C3	0000	00F0		% RESTORE A3	01727C00	
00D5	5C09	EC40	1000	00F0		% RESTORE A3	01728C00	
00D6	48C9	C0C0	4800	00F0		% RESTORE A3	01729C00	
00D7	1000	C0C0	0000	00F0		% RESTORE A3	01730C00	


```

0024 8809 2C32 001C 00F0
0529 0100 0030 00F0 00E0
052A 8809 2C32 0000 00F0
052B 0200 0000 0030 00E0
052C 6819 0009 0030 00F0
052D 4809 A0C1 0000 00F0
052E 8809 2C32 001C 00F0
052F 0100 0000 0000 00E0
0530 1820 A0C1 0000 00F0

0531 8809 0640 0030 00F0
0532 8809 20C3 001C 00F0
0533 0260 0000 0000 00E0
0534 2F30 0009 0000 00E0
0535 8809 0C40 0030 00F0
0536 2F30 0000 0030 00E0
0537 2F30 0000 0030 00E0
0538 8809 0C40 2F00 00F0
0539 8809 0F45 001C 00F0
053A 2F30 0003 0000 00E0
053B 8809 0C40 1000 00F0
053C 8809 20C3 001C 00F0
053D 2F30 0000 0030 00E0
053E 8809 0C40 0030 00F0
053F 8809 0C40 0030 00F0
0540 8809 0003 0030 00F0
0541 1820 0003 0000 00F0

0542 8809 0640 0030 00F0
0543 8809 20C3 001C 00F0
0544 0200 0000 0000 00E0
0545 2F30 0000 0000 00E0
0546 8809 0C40 0030 00F0
0547 0030 0000 2000 00F0
0548 0030 0000 0000 00E0
0549 8809 C0C0 A030 00F0
054A 8809 C131 2030 00F0
054B 8809 C131 2030 00F0
054C 8809 A0C3 0000 00F0
054D 8809 A0C1 4030 00F0
054E 8809 AC5C 4030 00F0
054F 8809 880E 4030 00F0
0550 0A00 0000 0030 00F0
0551 8809 0C40 0030 00F0
0552 8809 A000 C030 00F0
0553 0000 0000 0030 00E0
0554 8809 A0C1 4030 00F0
0555 8809 E0C3 8030 00F0
0556 8809 AC5C 4000 00F0
0557 8809 E0C3 0030 00F0
0558 8809 0000 0000 00F0
0559 883F 0000 0000 00F0

LIT + U = MARZ
16 = LIT
LIT EOL B
32 = LIT
IF TRUE THEN SKIP
A1 C = A1 J JUMP
LIT = MAR2
16 = LIT
A1 C = A1 J JUMP

AMPCR = MIR
LIT + 1 = MAR2
WORKSPACE = LIT
EINPUT - 1 = CPCR
B = A1
EINPUT + 1 = MAR2
EINPUT - 1 = CPCR
EINPUT + 1 = MAR2
EINPUT - 1 = CPCR
R = A3
LIT = MAR2
EINPUT - 1 = CPCR
P = MIR+BHI
B = AMPCR+BHI
STEP
JUMP

AMPCR = MIR
LIT = MAR2
PSW = LIT
EINPUT - 1 = CPCR
B = MIR+BHI
LIT = A2
LIT + 2 = LIT
A2 R = A2
A2 + LIT L = A2
A2 OR B = A3
A1 R = A1
A1 L = A1, BHI
A1 OR B = A1
A1 AND B011 = A1
IFETCH - 1 = CPCR
B = MIR
A1 R = A1
16 = SAR
A1 L = A1
A3 R = B
A3 OR B = A1+BHI
A3 = AMPCR
STEP
RETN

% THIS ROUTINE RESTORES THE REGISTERS
% OF THE LU IN WORKSPACE
% SAVE RETURN IN MIR
% MAR2 = WORKSPACE + 1

% RESTORE A1
% INCREMENT WORKSPACE ADDR
% RESTORE A2
% INCREMENT WORKSPACE ADDR
% RESTORE A3
% SELECT WORKSPACE BASE ADDR
% SWAP B AND MIR
% RESTORE AMPCR AND B

% THIS ROUTINE WILL PLACE THE CONTENTS
% OF PSW INTO THE PAR, THEN RESTORE
% THE PAR TO (PAR) + 2.
% SAVE RETURN ADDR TO OPCCOE IN MIR
% ADDRESS OF PSW

% (PSW) INTO B
% (PSW) INTO MIR, RETURN ADDR INTO 9
% PAR INTO A2
% RIGHT JUSTIFY (PAR)
% (PAR) + 2 = A2
% (PAR)+2/RETURN ADDR = A3
% CLEAR PAR

% (PSW) INTO PAR
% CLEAR BIASED FETCH BIT
% INSTRUCTION AT Y INTO B
% CLEAR PAR

% (PAR) + 2 = F
% RESTORE RETURN ADDR, INSTR IN B

```


055A	4809	0000	0000	0000	0	% THIS ROUTINE COMPUTES (P)*D = P	01916000
055B	4809	EC01	1C00	4000	0	% AND JUMPS TO NEXT INSTRUCTION	01920000
055C	3000	0000	0000	0000	0	% EXAMINE SIGN BIT OF *D*	01921000
055D	4809	0000	0000	0000	0	% A3 TO THE ADDR	01922000
055E	4C09	0019	0B00	0000	0	% IF HST THEN B111 L = B % IF SIGN=1, FILL UPPER BYTE WITH 1'S	01924000
055F	4809	0000	0000	0000	0	% RESTORE *D* FIELD TO LS BYTE	01925000
0560	4809	EC00	0000	0000	0	% B = SIGN/*D*, IN MS WORD	01926000
0561	0000	0000	0000	0000	0	% SAVE THE OLD PAR IN MS WORD OF A3	01928000
0562	4809	AD01	1C00	0000	0	% ALGEBRAICALLY ADD (P) + D	01930000
0563	4809	EC00	0000	0000	0	% CLEAR OLD PAR	01931000
0564	4809	AD00	0000	0000	0	% CREATE NEW PAR	01932000
0565	4809	AD01	1C00	0000	0	% THIS ROUTINE GETS THE CONTENTS OF RCM	01933000
0566	4809	AD00	0000	0000	0	% RCM INDICATED IN PAR AND RETURNS	01934000
0567	0A0C	0000	0000	0000	0	% REFERENCE PAR2	01935000
						% SAVE RETURN ADDRESS	01940000
						% SELECT REGISTER STACK TO RC USED	01941000
0568	5100	0000	0000	0000	0	% ADDR OF GEN REG STACK RETURNED IN PAR2	01942000
						% GET CONTENTS OF RCM	01943000
0569	2F30	0000	0000	0000	0	% RESTORE RETURN ADDRESS	01944000
056A	4809	CC00	0000	0000	0	% RIR IS USED AS TEMP STORAGE	01945000
056B	4809	0C00	0000	0000	0	% FOR TEST PURPOSES	01946000
056C	4800	0000	0000	0000	0	% THIS ROUTINE ANALYZES THE *M* FIELD OF	01947000
056D	4820	0000	0000	0000	0	% A TYPE RX INSTRUCTION. UPON ENTRANCE	01948000
						% A3 CONTAINS THE MOST SIGNIF. WORD OF	01949000
						% THE DOUBLEWORD INSTRUCTION. LC2	01950000
						% INDICATES BYTE INSTRUCTION. UPON EXIT	01951000
						% OF DAWI, DAWCI, OR INSTRUCTION	01952000
						% R CONTAINS YR LC2 PASSES MS(C)*LS(L)	01953000
						% PREPARE PS 2 BYTES OF A3 TO HOLD RETURN	01954000
						% ADDRESS UPON ADDR IN A3(UPPER HALF)	01955000
						% RESTORE A3 RETURN ADDR/INSTRUCTION	01956000
						% MASK OFF *M* FIELD	01957000
						% IS M = 0?	01958000
						% JUMP TO DIRECT ADDRESS W/O INDEXING	01959000
						% TEST FOR H = 1XXX	01960000
						% IF FALSE THEN STEP ELSE SKIP	01961000
						% JUMP TO DIRECT ADDR WITH INDEXING	01962000
						% IF TRUE THEN STEP ELSE SKIP	01963000
						% IF FALSE THEN STEP ELSE SKIP	01964000
						% IF TRUE THEN STEP ELSE SKIP	01965000
						% IF FALSE THEN STEP ELSE SKIP	01966000
						% IF TRUE THEN STEP ELSE SKIP	01967000
						% IF FALSE THEN STEP ELSE SKIP	01968000
						% IF TRUE THEN STEP ELSE SKIP	01969000
						% IF FALSE THEN STEP ELSE SKIP	01970000
						% IF TRUE THEN STEP ELSE SKIP	01971000
						% IF FALSE THEN STEP ELSE SKIP	01972000
						% IF TRUE THEN STEP ELSE SKIP	01973000
						% IF FALSE THEN STEP ELSE SKIP	01974000
						% IF TRUE THEN STEP ELSE SKIP	01975000
						% IF FALSE THEN STEP ELSE SKIP	01976000
						% IF TRUE THEN STEP ELSE SKIP	01977000
						% IF FALSE THEN STEP ELSE SKIP	01978000
						% IF TRUE THEN STEP ELSE SKIP	01979000
						% IF FALSE THEN STEP ELSE SKIP	01980000
						% IF TRUE THEN STEP ELSE SKIP	01981000
						% IF FALSE THEN STEP ELSE SKIP	01982000
						% IF TRUE THEN STEP ELSE SKIP	01983000
						% IF FALSE THEN STEP ELSE SKIP	01984000
						% IF TRUE THEN STEP ELSE SKIP	01985000
						% IF FALSE THEN STEP ELSE SKIP	01986000
						% IF TRUE THEN STEP ELSE SKIP	01987000
						% IF FALSE THEN STEP ELSE SKIP	01988000
						% IF TRUE THEN STEP ELSE SKIP	01989000
						% IF FALSE THEN STEP ELSE SKIP	01990000
						% IF TRUE THEN STEP ELSE SKIP	01991000
						% IF FALSE THEN STEP ELSE SKIP	01992000
						% IF TRUE THEN STEP ELSE SKIP	01993000
						% IF FALSE THEN STEP ELSE SKIP	01994000
						% IF TRUE THEN STEP ELSE SKIP	01995000
						% IF FALSE THEN STEP ELSE SKIP	01996000
						% IF TRUE THEN STEP ELSE SKIP	01997000
						% IF FALSE THEN STEP ELSE SKIP	01998000
						% IF TRUE THEN STEP ELSE SKIP	01999000
						% IF FALSE THEN STEP ELSE SKIP	02000000


```

C582 0030 0000 C000 0000
C583 4809 0000 8000 0000
C584 0000 0000 0000 0000
C585 3809 0000 0000 0000
C586 4820 0000 0000 0000

IFETCH - 1 = CPCR
A3 R = AHPCR
16 = SAR
IF LC2
JUMP

DAND1:
IFETCH - 1 = CPCR
B = A2
A3 AND LIT = B
A3 LIT = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
IF LC2 THEN SET LC2
BYTESTEST - 1 = CPCR
A2 + B = B
A3 R = AHPCR
16 = SAR
STEP
JUMP

INDIR:
LIT = MAR2
STATUS2 = LIT
EINPUT - 1 = CPCR
A2 EOL LIT
B = LIT
IF FALSE THEN A2 EOL LIT SKIP
SRM14 = HPCR
IF FALSE THEN A2 EOL LIT SKIP
SRM12 = HPCR
12 = LIT
IF FALSE THEN SKIP
SRM14 - 1 = HPCR
SRM16 - 1 = HPCR

SRM10:
B101 C = A2
23 = SAR
A2 AND B = 9
B = SAR
SRMTEST - 1 = HPCR

SRM12:

```

```

% DIRECT ADDRESSING WITH INDEXING (R(M))
% THIS ROUTINE RETURNS Y IN D
% AND JUMPS TO CALLING ROUTINE
% OF RXHFELD
% B WAS Y
% RESTORE RETURN ADDR FROM RXHFELD
% CLEAR BYTE BIT, LC2=0, MSBYTE OF Y
% RETURN TO CALLING ROUTINE OF RXHFELD
% THIS ROUTINE FORMS Y = Y + (R(M))
% RETURNS Y IN B
% GET NEXT ADDRESS
% ZI HAS Y IN B
% RESTORE RELATIVE REG. NO.
% SELECT REG. STACK TO BE USED
% COMPUTED ACTUAL LOCATION IN MAR2
% ELSE SKIP
% B WAS (R(M))
% CHECK FOR BYTE INSTRUCTION
% RESTORE RETURN ADDR FROM RXHFELD
% RETURN TO CALLING ROUTINE OF RXHFELD
% THIS ROUTINE IS CALLED IF M=10,12,14,16 OF C1000
% LOAD ADDR OF SRM2 REGISTER INTO MAR2
% READ SRM2 INTO B TO USE SRM ROUTINES
% TEST IF M = 10
% JUMP TO SRM2 "M" FIELD ROUTINE
% TEST IF M = 12
% TEST IF M = 14
% DEFAULTS TO M = 16
% THIS ROUTINE WILL REMOVE THE "M" FIELD
% FROM SRM2 AND CALL THE APPROPRIATE
% INDIRECT ADDRESSING ROUTINE
% ISOLATE "M" FIELD = 10
% B CONTAINS STATUS REG 2
% JUMP TO TEST CONTENTS ROUTINE
% THIS ROUTINE WILL REMOVE THE "M" FIELD

```

```

C1929000 0
C1980000 0
C1981000 0
C1982000 0
C1983000 0
C1984000 0
C1985000 0
C1986000 0
C1987000 0
C1988000 0
C1989000 0
C1990000 0
C1991000 0
C1992000 0
C1993000 0
C1994000 0
C1995000 0
C1996000 0
C1997000 0
C1998000 0
C1999000 0
C2000000 0
C2001000 0
C2002000 0
C2003000 0
C2004000 0
C2005000 0
C2006000 0
C2007000 0
C2008000 0
C2009000 0
C2010000 0
C2011000 0
C2012000 0
C2013000 0
C2014000 0
C2015000 0
C2016000 0
C2017000 0
C2018000 0
C2019000 0
C2020000 0
C2021000 0
C2022000 0
C2023000 0
C2024000 0
C2025000 0
C2026000 0
C2027000 0
C2028000 0
C2029000 0
C2030000 0
C2031000 0
C2032000 0
C2033000 0
C2034000 0
C2035000 0
C2036000 0
C2037000 0

```



```

05A7 4809 18C1 A030 00F0
05A8 9000 0000 0030 002C
05A9 4809 CC56 8830 00F0
05AA 2000 0000 0070 0010
05AB 08AC 0000 0030 0040

SRM14:
0101 C = A2
21 = SAR
A2 AND 0 R = 0
10 = SAR
SMTEST - 1 = MPCR

0101 C = A2
19 = SAR
A2 AND 0 R = 0
12 = SAR
SMTEST - 1 = MPCR

SRM16:
05B1 4809 18C1 A030 00F0
05B2 1C00 0000 0030 0020
05B3 4809 CC56 8830 00F0
05B4 A000 0000 0070 0010
05B5 0800 0000 0030 0040

05B6 4809 CC5E 0030 00F0
05B7 3010 0000 0000 00E0
05B8 7419 2C52 0040 00F0
05B9 386C 0000 0030 0040
05BA 4820 0000 0070 0010
05BB 0800 0000 0030 0040
05BC 491C 0000 0070 0040
05BD 4100 0000 0030 0040

05BE 4809 0003 0030 24F0
05BF 4809 0C40 0030 00F0
05C0 4809 0640 0800 00F0
05C1 4809 2003 0C1C 00F0
05C2 026C 0000 0030 00E0
05C3 2F5C 00C3 0070 0060
05C4 4809 0F45 001C 00F0
05C5 4809 A0C0 0030 00F0
05C6 2F50 00C0 0030 0060
05C7 4809 0F46 001C 00F0
05C8 4809 0000 0030 00F0
05C9 2F50 00C3 0070 0060
05CA 4809 0F46 001C 00F0
05CB 4809 5000 0030 00F0
05CC 2F50 00C3 0070 0060
05CD 4809 0C40 004C 00F0
05CE 4809 0003 0030 00F0

SRM14:
0101 C = A2
21 = SAR
A2 AND 0 R = 0
10 = SAR
SMTEST - 1 = MPCR

0101 C = A2
19 = SAR
A2 AND 0 R = 0
12 = SAR
SMTEST - 1 = MPCR

SRM16:
05D1 4809 18C1 A030 00F0
05D2 1C00 0000 0030 0020
05D3 4809 CC56 8830 00F0
05D4 A000 0000 0070 0010
05D5 0800 0000 0030 0040

05D6 4809 CC5E 0030 00F0
05D7 3010 0000 0000 00E0
05D8 7419 2C52 0040 00F0
05D9 386C 0000 0030 0040
05DA 4820 0000 0070 0010
05DB 0800 0000 0030 0040
05DC 491C 0000 0070 0040
05DD 4100 0000 0030 0040

05DE 4809 0003 0030 24F0
05DF 4809 0C40 0030 00F0
05E0 4809 0640 0800 00F0
05E1 4809 2003 0C1C 00F0
05E2 026C 0000 0030 00E0
05E3 2F5C 00C3 0070 0060
05E4 4809 0F45 001C 00F0
05E5 4809 A0C0 0030 00F0
05E6 2F50 00C0 0030 0060
05E7 4809 0F46 001C 00F0
05E8 4809 0000 0030 00F0
05E9 2F50 00C3 0070 0060
05EA 4809 0F46 001C 00F0
05EB 4809 5000 0030 00F0
05EC 2F50 00C3 0070 0060
05ED 4809 0C40 004C 00F0
05EE 4809 0003 0030 00F0

```


[illegible]

[illegible]


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0650 4809 00C1 0000 0000 0 02278C00 0
0651 4809 0000 0000 0000 0 02279C00 0
0652 4809 2045 0000 0000 0 02280C00 0
0653 4809 0003 0000 0000 0 02281C00 0
0654 4809 0000 0000 0000 0 02282C00 0
0655 4809 0F42 0035 0000 0 02283C00 0
0656 0800 00C0 0030 0000 0 02284C00 0
0657 4809 0F43 801C 0000 0 02285C00 0
0658 0800 00C0 0030 0020 0 02286C00 0
0659 4809 00C0 0030 0000 0 02287C00 0
065A 4809 0F40 200F 0000 0 02288C00 0
065B 4809 0C43 001C 0000 0 02289C00 0
065C 4809 C000 0000 0000 0 02290C00 0
065D 4809 00C0 0000 0000 0 02291000 0
065E 4809 0040 2030 0000 0 02292C00 0
065F 4809 1803 8800 0000 0 02293C00 0
0660 00C0 00C0 0030 0020 0 02294C00 0
0661 20C8 8000 0030 0000 0 02295C00 0
0662 4809 C05C 203C 0000 0 02296C00 0
0663 4809 C0C0 0030 0000 0 02297000 0
0664 3809 0000 0030 1000 0 02298C00 0
0665 3008 00C0 0000 1000 0 02299C00 0
0666 4809 C155 2000 0000 0 02300C00 0
0667 00FC 00C0 0030 0000 0 02301000 0
0668 4809 C043 0030 0000 0 02302C00 0
0669 4809 C050 201C 0000 0 02303C00 0
066A 4809 C050 0030 0000 0 02304C00 0
066B 0000 00C0 0030 0020 0 02305C00 0
066C 20C8 C000 C030 0000 0 02306C00 0
066D 5260 00C0 0030 0000 0 02307000 0
066E 5130 C000 0000 C000 0 02308C00 0

% GENERATE 512 IN B
% B NOW CONTAINS 768(ADDR OF PAGEREG)
% REFERENCE BR2
% SAVE HARGOFFECT IN COUNTER
% PUT BR2(PAGE ADDR REG NO.) IN MAR2
% SAVE A2 IN MIR
% USE A2 AS X-SELECT INCLDFF FOR BRAR
% MAR2 CONTAINS THE BASE ADDRESS OF THE
% DESIRED PAGE ADDRESS REGISTER
% READ CONTENTS OF PAGE ADDR. REG.
% READ COMPLETE STORE IN E
% SAVE PAGE ADDRESS REG CONTENTS IN A2
% SET PAGE MODIFICATION BIT (BIT 15)
STEP ELSE SKIP % STORE TO MEMORY, SET
% PAGE REFERENCED BIT IN PAGE ADDR REG
% FORM PAGE ADDRESS REG PLUS MOD. BIT
% SAVE RETURN IN R
% MODIFIED PAGE ADDR. REG. IN MIR
% WRITE OUT MODIFIED PAGE REG
% ISOLATE PAGE NUMBER
% MASK OFF LOW 8 BITS
% RESTORE A2
% R HAS THE PAGE REG. CONTENTS
% BR2 CONTAINS DIRECT ADDRESS (PAGEINC
% COMPLETE)
% SET IN COUNTER
% RETURN TO EMLIN
%
%
% ***** OFCODE IMPLEMENTATION *****
%
% THIS ROUTINE WILL FETCH AN INSTRUCTION
% ANALYZE THE OP(CODE(UPPER 6 BITS) AND(2318C00 0
% SELECT THE CORRESPONDING ROUTINE FOR
% THE SELECTED OPERATION.
% A1 TO THE ADDR
% A1 EXAMINE REPOTE EXECUTE BIT
% GET THE NEXT INSTRUCTION
% CLEAR CONDITION BITS
% SAVE INSTRUCTION INTO A3
% PLACE THE 6 OP(CODE BITS IN LOW ORDER 6
% BITS OF A2
% CREATE ADDRESS OF OPERATION ROUTINE
% BASE ADDRESS OF OPTABLE
% SETTING OFCODE VALUE TO OPTABLE BASE
% JUMP TO AMPCR + 1
%
% THE FOLLOWING 64 INSTRUCTIONS CORRESPOND TO SUPROUTINE CALLS TO THE

```


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2 6
3 6
4 6
5 6
6 6
7 6
8 6
9 6

1 A1 CONTAINS THE PSW
2 A2 SERVES AS A TEMPORARY REGISTER
3 FOR RETURNS, ETC.
4 P IS THE WORKING REGISTER
5 A3 CONTAINS THE INSTRUCTION

2 6
3 6
4 6
5 6
6 6
7 6
8 6
9 6

06C7C	06C30	00FC3	000FC	0040	1	MF	CR
06C7D	06C31	00FC3	000FC	0040	1	MF	CR
06C7E	06C32	00FC3	000FC	0040	1	MF	CR
06C7F	06C33	00FC3	000FC	0040	1	MF	CR
06C80	06C34	00FC3	000FC	0040	1	MF	CR
06C81	06C35	00FC3	000FC	0040	1	MF	CR
06C82	06C36	00FC3	000FC	0040	1	MF	CR
06C83	06C37	00FC3	000FC	0040	1	MF	CR
06C84	06C38	00FC3	000FC	0040	1	MF	CR
06C85	06C39	00FC3	000FC	0040	1	MF	CR
06C86	06C3A	00FC3	000FC	0040	1	MF	CR
06C87	06C3B	00FC3	000FC	0040	1	MF	CR
06C88	06C3C	00FC3	000FC	0040	1	MF	CR
06C89	06C3D	00FC3	000FC	0040	1	MF	CR
06C8A	06C3E	00FC3	000FC	0040	1	MF	CR
06C8B	06C3F	00FC3	000FC	0040	1	MF	CR
06C8C	06C40	00FC3	000FC	0040	1	MF	CR
06C8D	06C41	00FC3	000FC	0040	1	MF	CR
06C8E	06C42	00FC3	000FC	0040	1	MF	CR
06C8F	06C43	00FC3	000FC	0040	1	MF	CR
06C90	06C44	00FC3	000FC	0040	1	MF	CR
06C91	06C45	00FC3	000FC	0040	1	MF	CR
06C92	06C46	00FC3	000FC	0040	1	MF	CR
06C93	06C47	00FC3	000FC	0040	1	MF	CR
06C94	06C48	00FC3	000FC	0040	1	MF	CR
06C95	06C49	00FC3	000FC	0040	1	MF	CR
06C96	06C4A	00FC3	000FC	0040	1	MF	CR
06C97	06C4B	00FC3	000FC	0040	1	MF	CR
06C98	06C4C	00FC3	000FC	0040	1	MF	CR
06C99	06C4D	00FC3	000FC	0040	1	MF	CR
06C9A	06C4E	00FC3	000FC	0040	1	MF	CR
06C9B	06C4F	00FC3	000FC	0040	1	MF	CR
06C9C	06C50	00FC3	000FC	0040	1	MF	CR
06C9D	06C51	00FC3	000FC	0040	1	MF	CR
06C9E	06C52	00FC3	000FC	0040	1	MF	CR
06C9F	06C53	00FC3	000FC	0040	1	MF	CR
06CA0	06C54	00FC3	000FC	0040	1	MF	CR
06CA1	06C55	00FC3	000FC	0040	1	MF	CR
06CA2	06C56	00FC3	000FC	0040	1	MF	CR
06CA3	06C57	00FC3	000FC	0040	1	MF	CR
06CA4	06C58	00FC3	000FC	0040	1	MF	CR
06CA5	06C59	00FC3	000FC	0040	1	MF	CR
06CA6	06C5A	00FC3	000FC	0040	1	MF	CR
06CA7	06C5B	00FC3	000FC	0040	1	MF	CR
06CA8	06C5C	00FC3	000FC	0040	1	MF	CR
06CA9	06C5D	00FC3	000FC	0040	1	MF	CR
06CAA	06C5E	00FC3	000FC	0040	1	MF	CR
06CAB	06C5F	00FC3	000FC	0040	1	MF	CR
06CAC	06C60	00FC3	000FC	0040	1	MF	CR
06CAD	06C61	00FC3	000FC	0040	1	MF	CR
06CAE	06C62	00FC3	000FC	0040	1	MF	CR
06CAF	06C63	00FC3	000FC	0040	1	MF	CR
06CAG	06C64	00FC3	000FC	0040	1	MF	CR
06CAH	06C65	00FC3	000FC	0040	1	MF	CR
06CAI	06C66	00FC3	000FC	0040	1	MF	CR
06CAJ	06C67	00FC3	000FC	0040	1	MF	CR
06CAK	06C68	00FC3	000FC	0040	1	MF	CR
06CAL	06C69	00FC3	000FC	0040	1	MF	CR
06CAM	06C6A	00FC3	000FC	0040	1	MF	CR
06CAN	06C6B	00FC3	000FC	0040	1		

2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463	2464	2465	2466
------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------


```

040C 1080 0009 0000 0040
040D 1090 0009 0030 0040

0F012 - 1 = MPCR
0F013 - 1 = MPCR

0F010:
060E 4809 2C55 0000 00FC
060F 00F0 0000 0070 00FC
0610 31CC 00C3 0000 0060

0611 2F30 0000 0000 0060
0612 4809 0040 0030 0060
0613 200C 0000 007C 0060
0614 4809 00C0 0070 0060
0615 80FC 00C3 0000 0080
0616 4809 0055 0030 0060
0617 51CC 00C3 0070 0060

0618 2F50 0000 0000 0060
0619 56E0 0000 007C 0040

0F011:
061A 4809 2C55 0030 00FC
061B 00F0 0000 0070 00FC
061C 51CC 00C3 0000 0060

061D 2F30 0000 0010 0060
061E 4809 0C41 0010 00FC
061F 00C0 0000 0000 0030
0620 60E0 0000 0070 0060
0621 4809 0C40 0030 0060
0622 200C 0000 0000 0060
0623 4809 00C0 0000 00FC
0624 90F0 00C0 0030 0080
0625 4809 2C55 0030 00FC
0626 51CC 00C3 0000 0060

0627 2F50 0000 0000 0060
0628 56E0 00C0 007C 0040

0F012:
0629 6130 00C0 0030 0060
062A 4809 00C1 1000 00FC
062B 00F0 0000 0030 0040
062C 4809 0C5C 1000 00FC
062D 4809 00C0 0070 0060
062E 4809 00C0 0000 00FC
062F 4809 0156 001C 00FC
0700 4809 0F52 0000 00FC
0701 600B 0000 0070 00FC
0702 5670 0000 0000 0060
0703 4809 00C1 2000 0060
0704 000C 0000 0000 0020
0705 4809 0000 0000 00FC
0706 4809 00C0 0030 00FC
0707 200C 0000 0000 0060

02458000 0
02458000 0
02458000 0
02461000 0
02461000 0
02462000 0
02463000 0
02464000 0
02465000 0
02466000 0
02467000 0
02468000 0
02469000 0
02470000 0
02471000 0
02472000 0
02473000 0
02474000 0
02475000 0
02476000 0
02477000 0
02478000 0
02479000 0
02480000 0
02481000 0
02482000 0
02483000 0
02484000 0
02485000 0
02486000 0
02487000 0
02488000 0
02489000 0
02490000 0
02491000 0
02492000 0
02493000 0
02494000 0
02495000 0
02496000 0
02497000 0
02498000 0
02499000 0
02500000 0
02501000 0
02502000 0
02503000 0
02504000 0
02505000 0
02506000 0
02507000 0
02508000 0
02509000 0
02510000 0
02511000 0
02512000 0
02513000 0
02514000 0
02515000 0
02516000 0
02517000 0

% RR TYPE INSTRUCTION
% CONTENTS OF R(H) STORED INTO R(A)
% SELECT LS 4 BITS OF B (*#* FIELD)
% SELECT REGISTER STACK TO BE USED
% ADDR OF GEN REG STACK RETURNED IN MAR2
% PUT CONTENTS OF R(H) IN B
% CONTENTS OF R(H) IN MIR
% ARITHMETIC CC SETTING (CENTER WITH B)
% OBTAIN *A* FIELD
% SELECT REGISTER STACK TO BE USED
% ADDR OF GEN REG STACK RETURNED IN PAR2
% CONTENTS OF R(H) INTO R(A)
%
% RI TYPE IT, (Y*) INTO R(A)
% OBTAIN INE *#* FIELD
% SELECT REGISTER STACK TO BE USED
% ADDR OF GEN REG STACK RETURNED IN MAR2
% R(CH) = Y* PUT INTO D
% SET UP ADDRESS OF Y* IN ER2
% READ (Y*) INTO B
% (Y*) IN MIR
% ARITHMETIC CC SETTING (CENTER WITH B)
% EXTRACT *A* FIELD
% SELECT REGISTER STACK TO BE USED
% ADDR OF GEN REG STACK RETURNED IN MAR2
% WRITE OUT CONTENTS OF Y* INTO R(A)
%
% RK TYPE INSTRUCTION
% (Y) INTO R(A) IF B = 0
% (Y) R(CH) = R(A) IF B# 0
% GET CONTENTS OF Y* FIELD
% PREPARE A3 FOR STORAGE OF Y* FIELD
% CLEAR MIR, BR2,
% PLACE Y* FIELD IN LS 4 BITS OF A2
% PUT Y* FIELD INTO MAR
% CHECK IF *#* FIELD 0
% SKIP
% ANALYZE R(H) AND RETURN VALUE IN MIR
% ISOLATE Y INTO A2
% PUT Y INTO A2 AND R(CH) INTO B
% B, MIR CONTAINS FUTURE CONTENTS OF R(A)
% ARITHMETIC CC SETTING (CENTER WITH B)

```



```

0708 4809 0000 0030 0000
0709 0000 0000 0000 0000
070A 4809 2C55 0030 0000
070B 5100 0000 0030 0000
070C 2F5C 0000 0030 0000
070D 660C 0000 0030 0000

070E 5700 0000 0000 0000
070F 4809 0000 0030 0000
0710 0000 0000 0000 0000
0711 600C 0000 0000 0000
0712 4809 0000 0000 0000
0713 2000 0000 0000 0000
0714 4809 0000 0000 0000
0715 800C 0000 0000 0000
0716 4809 2C55 0030 0000
0717 510C 0000 0000 0000

0718 2F5C 0000 0000 0000
0719 660C 0000 0000 0000

071A 2809 0000 0000 0000
071B 3809 0000 0000 0000
071C 5F50 0000 0000 0000
071D 4809 0000 0000 0000
071E 100C 0000 0000 0000
071F 4809 0000 0000 0000
0720 4824 0000 0000 0000

0721 100C 0000 0000 0000
0722 100C 0000 0000 0000
0723 300C 0000 0000 0000
0724 1000 0000 0000 0000

0725 4009 0000 0000 0000
0726 500C 0000 0000 0000
0727 4809 2C55 0030 0000
0728 510C 0000 0000 0000
0729 2F5C 0000 0000 0000
072A 4809 0000 0000 0000
072B 000C 0000 0000 0000
072C 4809 0000 0000 0000
072D 100C 0000 0000 0000
072E 4809 0000 0000 0000
072F 000C 0000 0000 0000
0730 7800 0000 0000 0000
0731 3000 0000 0000 0000
0732 1824 0000 0000 0000

0733 100C 0000 0000 0000
0734 1100 0000 0000 0000
0735 1100 0000 0000 0000

```

```

* PUT 1A: FIELD INTO 4 BITS OF 0
* PUT 400P OF 4(A) INTO 0
* SELECT REGISTER STACK TO BE USED
* ADDR OF GEN REG STACK RETURNED IN MAR2
* (RCH) + (Y) INTO 6(A)
* GET NEXT INSTRUCTION
* RX TYPE INSTRUCTION
* (Y) INTO 6(A)
* ANALYZE "M" FIELD CONTENTS
* ISOLATE Y INTO BR2
* (Y) INTO B
* STORE (Y) INTO MIR
* ARITHMETIC CC SETTING (ENTER WITH B)
* ISOLATE 1A: FIELD
* SELECT REGISTER STACK TO BE USED
* ADDR OF GEN REG STACK RETURNED IN MAR2
*
* THIS ROUTINE DECODES THE 02 OPCODE
* CLEARS LOCAL COMP. BITS
*
* UNARY FUNCTION DESCRIPTION
* 1H: FIELD SELECTS UNARY INST.
* ISOLATE 1A: FIELD
*
* B = B
* 4 = SAR; 15 = LIT
* LIT AND B = B
* REGSTACK - 1 = CPCR
* INPUT - 1 = CPCR
* A3 AND LIT = A2
* A3 = LIT
* A3 = AMPCR
* 0P02M - 1 = AMPCR
* A2 CERO LIT
* 12 = LIT
* IF TRUE THEN STEP ELSE SKIP
* FAULT - 1 = MPCR
* EXEC
*
* 0P013:
*
* 0P020:
*
* 0P0201:
*
* 0P0201:
*
* 0P0201:
*
* 0P020H:

```



```

07C6 4809 2001 0820 00F0
07C7 4809 CC40 0C30 00F0
07C8 78C9 00C0 0090 00F0
07C9 1E7C 00C0 0000 0060
07CA 4F1C 00C0 0030 0060
07CB 4809 00C0 0090 00F0
07CC 4809 0C40 8B30 00F0
07CD 00C0 00C0 0090 0020
07CE 200C 00C0 0090 0060
07CF 2F5F 00C0 0000 0060
07D0 66EC 00C0 0030 0040

07D1 4809 0C40 2C4C 00F0
07D2 0020 00C0 00C0 0040
07D3 4809 2001 0820 00F0
07D4 4809 CC5E 0030 00F0
07D5 78C9 00C0 0000 0060
07D6 1E7C 00C0 00C0 0060
07D7 4F1C 00C0 0030 0060
07D8 48C9 00C0 0000 00F0
07D9 4809 0C40 8B30 00F0
07DA 00C0 00C0 0090 0020
07DB 200C 00C0 0090 0060
07DC 2F5F 00C0 0000 0060
07DD 66EC 00C0 0030 0040

07DE 4809 2C55 0830 00F0
07DF 00F0 00C0 00C0 00E0
07E0 51C0 00C0 0030 0060
07E1 2F3C 00C0 00C0 0060
07E2 48C0 00C0 0030 0060
07E3 66EC 00C0 0030 0040

07E4 570C 00C0 00C0 0060
07E5 4820 00C0 0020 0060
07E6 56E0 00C0 0C30 004C

07E7 5F9C 00C0 00C0 0060
07E8 4809 CC40 0040 00FC
07E9 118C 00C0 0030 00CC
07EA 48C9 00C0 0000 00F0
07EB 4824 00C0 0030 00F0

07EC 11C0 07C0 00C0 0040
07ED 300C 00C0 0C3C 0040
07EE 300C 07C0 00C0 0040
07EF 11D0 C0C0 0C30 0040

07F0 4809 2C56 2030 00F0
07F1 00FC 00C0 0030 00E0
07F2 48C9 C640 0030 00FC
07F3 11EC 00C0 0030 00CC

```

```

LIT L = 0
A2 + B = MIR
IF ADV THEN SET LC1
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
BMI
B R = B+MIR
B = SAR
SETCCA - 1 = CPCR
EUTPUT - 1 = CPCR
OPCODE - 1 = HPCR

0P02013:
B L = A2
COMP L6 = SARJ 2 = LITR (BCA) IN UNW OF A2
LIT L6 = 9J SET LC2
A2 - B = MIR
IF ADV THEN SET LC1
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
BMI
B R = B+MIR
B = SAR
SETCCA - 1 = CPCR
EUTPUT - 1 = CPCR
OPCODE - 1 = HPCR

0P021:
B AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
LDBLE - 1 = CPCR
OPCODE - 1 = HPCR

0P023:
B+MFIELD - 1 = CPCR
LDBLE - 1 = CPCR
OPCODE - 1 = HPCR

0P0CODE03:
XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP03F - 1 = AMPCR
STEP
EXEC
OP03C - 1 = HPCR
FAULT - 1 = MPCR
FAULT - 1 = MPCR
OP033 - 1 = MPCR

B AND LIT = A2
15 = LIT
A2 + AMPCR = AMPCR
OP030H - 1 = AMPCR

```

```

% CHECK FOR CARRY
% CHECK FOR OVERFLOW
% RESULT IN LNW OF B+MIR
% DECREASE RA BY TWOJ TYPE RR
% (RA) - 2 -> RA
% B = (RA)J MAR2 = RA
% LC2 IS SUBTRACTION FLAG
% SET/CLEAR CARRY BIT
% CHECK FOR OVERFLOW
% RESULT IN LNW OF B AND MIR
% LOAD DOUBLE TYPE R(C11)
% (Y+Y+1) -> RA+RA+1J SET CC
% ISOLATE IN: FIELD
% B = (REM) = Y+
% CALL LOAD DOUBLE ROUTINE
% LOAD DOUBLEJ TYPE RX
% (Y+Y+1) -> RA+RA+1
% CALL LOAD DOUBLE ROUTINE
% THIS ROUTINE ANALYZES THE 03 OPCODE

```

```

02755C00 0
02756C00 0
02761C00 0
02762C00 0
02763C00 0
02764C00 0
02765C00 0
02766C00 0
02767C00 0
02768C00 0
02769C00 0
02770C00 0
02771C00 0
02772C00 0
02773C00 0
02774C00 0
02775C00 0
02776C00 0
02777C00 0
02778C00 0
02779C00 0
02780C00 0
02781C00 0
02782C00 0
02783C00 0
02784C00 0
02785C00 0
02786C00 0
02787C00 0
02788C00 0
02789C00 0
02790C00 0
02791C00 0
02792C00 0
02793C00 0
02794C00 0
02795C00 0
02796C00 0
02797C00 0
02798C00 0
02799C00 0
02800C00 0
02801C00 0
02802C00 0
02803C00 0
02804C00 0
02805C00 0
02806C00 0
02807C00 0
02808C00 0
02809C00 0
02810C00 0
02811C00 0
02812C00 0
02813C00 0
02814C00 0
02815C00 0
02816C00 0
02817C00 0

```


168


```

0823 4809 E000 9000 0000
0824 4050 0000 0000 0000
0825 4809 E150 0000 0000
0826 5100 0000 0000 0000
0827 2F30 0000 0000 0000
0828 4809 A000 0000 0000
0829 0000 0000 0000 0000
082A 4809 A001 4000 0000
082B 4809 AC5C 4000 0000
082C 5600 0000 0000 0000

```

0P030051:

```

082D 4809 E000 9000 0000
082E 4809 E150 0000 0000
082F 5100 0000 0000 0000
0830 5100 0000 0000 0000
0831 2F30 0000 0000 0000
0832 4809 0C41 0000 0000
0833 0000 0000 0000 0000
0834 4809 2001 2000 0000
0835 307C 0000 0000 0000
0836 4809 2001 0000 0000
0837 0700 0000 0000 0000
0838 4809 C5C0 0000 0000
0839 4809 0C42 2000 0000
083A 4809 C5C6 0000 0000
083B 4809 C002 0000 0000
083C 4809 AC5E 2000 0000
083D 4809 C5C0 0000 0000
083E 4809 AC01 4000 0000
083F 0000 0000 0000 0000
0840 4809 A000 0000 0000
0841 4809 AC5C 4000 0000
0842 5600 0000 0000 0000

```

0P030061:

```

0843 4809 E000 9000 0000
0844 307C 0000 0000 0000
0845 4809 E150 0000 0000
0846 2F30 0000 0000 0000
0847 2F30 0000 0000 0000
0848 4809 0C40 2000 0000
0849 4809 2003 0000 0000
084A 022C 0000 0000 0000
084B 2F30 0000 0000 0000
084C 4809 0C40 8000 0000
084D 0000 0000 0000 0000
084E 4809 0C41 0000 0000
084F 4809 C5C0 0000 0000
0850 2F50 0000 0000 0000
0851 5600 0000 0000 0000

```

0P0331:

```

0852 5330 0000 0000 0000
0853 4809 0C41 0000 0000
0854 0000 0000 0000 0000
0855 4809 EC5C 1000 0000

```

```

A3 R = A3
4 = SARI 15 = LIT
A3 AND LIT = B
REGSTACK - 1 = CPCR
EIINPUT - 1 = CPCR
A1 R = A1
16 = SAR
A1 L = A1
A1 OR B = A1
OPCODE - 1 = MPCR

% RA IN MAR2
% B = (R(A))

% ZERO PAR
% (R(A)) INTO P UPPER 16 BITS UNTOUCHED

%
%
% LOAD SRI ; (R(A)) INTO SRI
%
%
% RA IN MAR2
% B = (R(A))
% STORE (R(A)) IN UNW OF MIR
%
% CREATE BIT MASK FOR LOADER TOGGLES
%
% LOWER MASK OF SRI
%
% CREATE MASK ONES IN UNW GF B
% MASK FOR (RA)
% MASK OFF (RA), STORE IN MIR
% MASK FOR A1 (PEW)
% MASK OFF SAVED PART OF A1 INTO A2
% CREATE NEW A1 VALUE FROM (R(A))
% CLEAR UNW OF A1
%
% RESTORE A1
% RESTORE A1 (ACTIVE PSW)
% UNTOUCHED
%
% LOAD SR2; (R(A)) INTO SR2
%
% PA = MAR2
% B = (R(A))
% (R(A)) = A2
%
% R = (STATUS2)
% ISOLATE UPPER 16 BITS OF STATUS2
%
% NEW STATUS2 CREATED
% (R(A)) INTO STATUS2
%
%
% LOAD MULTIPLE, TYPE RX
% (Y ... Y + M - A + 1) INTO RA ... RH
% B = Y: = Y
%
% STORE Y IN UNW OF A3

```


0000 1200 0003 0000 0000
0000 1200 0003 0000 0000
0000 1200 0003 0000 0000

00000001

00000001 - 1 = MPCR
00000002 - 1 = MPCR
00000003 - 1 = MPCR

00000001 - 1 = MPCR
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00000001 - 1 = MPCR
00000002 - 1 = MPCR
00000003 - 1 = MPCR

00000001 - 1 = MPCR
00000002 - 1 = MPCR
00000003 - 1 = MPCR

00000001 - 1 = MPCR
00000002 - 1 = MPCR
00000003 - 1 = MPCR


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```

0P0401:

```

B R = B
4 = SAR, 15 = LIT
LIT AND 6 = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A3
0 = A2
14 = LIT
LCTR, SAVE
A3
IF LST THEN A2 OR 1 = A2, SKIP 1 INTO LSB OF A2
A2 AND B110 = A2
A3 R = A3*CSAR
1 = SAR
IF NOT COV THEN A2 L = A2*INC, JUMP
A2 = B*HIR - 1 = CPCR
EINPUT - 1 = CPCR
OPCODE - 1 = HPCR

```

0P0402:

```

B R = B
4 = SAR, 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
0 = A2*HIR
14 = LIT
LCTR, SAVE
B
IF LST THEN A2 + 1 = A2*HIR, % INCREMENT COUNTER
B R = B
1 = SAR
IF NOT COV THEN INC, JUMP
B*HAR + 1 = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
OPCODE - 1 = HPCR

```

0P0403:

```

B R = B
4 = SAR, 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR

```

```

% (RA+1)
% SORT INTO R(A+1)
% R(A)
% REMAINDER INTO R(A)
%
% RVRT REVERSE REGISTER, (REVERSE RA)
% 1A: FIELD LS BITS OF B
% B = 1A: FIELD
% RA = HAR2
% B = (R(A))
% ZERO A2
% EXECUTE LOOP 16 TIMES
% CNT, COUNT ONES, COUNT -> RA + 1
% 1A: FIELD LS BITS OF B
% RA=HAR2
% R = (R(A))
% ZERO COUNT REGISTER
% EXECUTE LOOP 16 TIMES
% SHIFT RA RIGHT
% R(A+1) INTO HAR2
% STORE COUNT IN HIR INTO RA + 1
% SFR, SCALE FACTOR, (RA*RA+1) SHIFTED
% LEFT UNTIL (R(A))15 NEG (R(A))14
% SHIFT COUNT -> RA+2
% 1A: FIELD INTO B
% RA = HAR2
% B = (R(A))

```



```

052C 5F90 00C0 0000 0060 03179C00 0
052D 4809 C440 0040 C0C0 03186C00 0
052E 1324 00C0 00C0 00C0 03181C00 0
052F 4809 00C0 0000 0060 03187C00 0
0530 4824 00C0 007C C0C0 03183C00 0
0531 133C 00C3 0000 0040 03184C00 0
0532 1340 00C3 0000 0040 03185C00 0
0533 3000 00C0 007C C040 03186C00 0
0534 133C 00C3 0000 0040 03187C00 0

0535 4809 0C43 88C0 0060 03191C00 0
0536 80F0 00C3 0000 0060 03192C00 0
0537 4809 2C55 0830 C0F0 03193C00 0
0538 51C0 0000 0070 C060 03194C00 0
0539 2F30 0003 0C70 C060 03195C00 0
053A 4809 0C40 2C00 00F0 03196C00 0
053B 4809 E156 0800 00F0 03197C00 0
053C 00F0 00C0 0000 00E0 03198C00 0
053D 4809 0C5E 0000 80F0 03199C00 0
053E 4809 0C51 0830 00F0 03200C00 0
053F 4809 C55C 089C 00F0 03201C00 0
0540 2F50 00C0 0070 C060 03202C00 0
0541 200C 0003 0070 0060 03203C00 0
0542 56E0 0C03 0000 0040 03204C00 0

0543 4809 2C55 0830 00F0 03205C00 0
0544 00F0 00C3 0000 00E0 03206C00 0
0545 51C0 00C3 0070 0060 03207C00 0
0546 2F30 00C0 0000 0060 03208C00 0

0547 4805 0C41 CC10 C0F0 03209C00 0
0548 0C00 00C0 009C C030 03210C00 0
0549 60C0 0003 0000 0060 03211C00 0
054A 4809 CC40 0030 00F0 03212C00 0
054B 1C80 00C0 009C 006C 03213C00 0
054C 51C0 00C0 0000 0060 03214C00 0
054D 2F50 00C0 0000 0060 03215C00 0
054E 4809 00C0 C000 C0F0 03216C00 0
054F 200C 0000 0000 0060 03217C00 0
0550 308B C000 0000 C0FC 03218C00 0
0551 56E0 0000 C070 C040 03219C00 0
0552 4809 C000 C800 0060 03220C00 0
0553 51C0 0000 0000 0060 03221C00 0
0554 2F3C 0000 0000 0060 03222C00 0
0555 4809 CC45 0030 00F0 03223C00 0
0556 2F50 0000 0000 0060 03224C00 0
0557 56E0 00C0 0000 0040 03225C00 0

0558 5700 00C0 0000 C060 03226C00 0
0559 946C 00C0 0000 C040 03227C00 0

```

```

OPCODE051
XFCODE - 1 = CPCR
A2 * AMPCR = AMPCR
OP05F - 1 = AMPCR
EXEC
OP05F1
OP05A - 1 = MPCR
OP05B - 1 = MPCR
FAULT - 1 = MPCR
OP053 - 1 = MPCR

OP0501
B R = B
4 = SARI 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A2
A3 AND LIT = B
15 = LIT
- B = SAR
8001 L = B
A2 OR B = MIR#B
EOUTPUT - 1 = CPCR
SETCCA - 1 = CPCR
OPCODE - 1 = MPCR

OP0511
LIT AND B = B
15 = LIT
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B L = RR2
COMP 8 = SAR
EYULIN - 1 = CPCR
B = MIR
A2OM - 1 = CPCR
REGSTACK - 1 = CPCR
EOUTPUT - 1 = CPCR
BHI
SETCCA - 1 = CPCR
IF LC2 THEN STEP ELSE SKIP % LC2 SET IN A2OM
OPCODE - 1 = MPCR
A2 = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
R + 1 = MIR
EOUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

LOINX11
B L = RR2
EYULIN - 1 = CPCR
A2OM - 1 = CPCR
REGSTACK - 1 = CPCR
EOUTPUT - 1 = CPCR
BHI
SETCCA - 1 = CPCR
IF LC2 THEN STEP ELSE SKIP % LC2 SET IN A2OM
OPCODE - 1 = MPCR
A2 = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
R + 1 = MIR
EOUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

OP0531
RYNFIELD - 1 = CPCR
EYULIN - 1 = MPCR
LOINX11 - 1 = MPCR

```

```

% THIS ROUTINE ANALYZES THE 05 OPCODE
% SBRJ SET BIT 1 -> (RCA)J
% B = 1A1 FIELD
% MAR2 = RA
% B = (RCA)
% B = 1M1 FIELD
% VARIABLE SHIFT AMOUNT FOR LEFT SHIFT
% SET 1 INTO (RCA)M AND STORE INTO MIR
% MODIFIED (RCA) -> RA
% LXIJ LOAD AND INDEX BY 1J
% TYPE RI(2)
% B = 1M1 FIELD
% MAR2 = R#
% (R#) = Y# = B
% B = (Y#) OR (Y)
% MIR = (Y#) OR (Y)
% IS A EQUAL M J B=A* A2 = M*
% RA = MAR2
% (Y) OR (Y#) -> RA
% (Y) OR (Y#) -> P
% (Y) OR (Y#) -> P
% MIR = (R#)
% MIR = (R#) + 1
% LXIJ LOAD AND INDEX BY 1J
% TYPE RI
% B = Y
% LOAD AND INDEX BY 1

```


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00000000000000000000000000000000

095A	5190	0003	0030	0030	0060
095B	4809	0640	0040	0040	0060
095C	1360	0000	0000	0000	0000
095D	4809	0000	0000	0000	0000
095E	4824	0000	0000	0000	0000
095F	1370	0000	0000	0000	0000
0960	1390	0000	0000	0000	0000
0961	3070	0000	0000	0000	0000
0962	1390	0000	0000	0000	0000
0963	4809	0000	0000	0000	0000
0964	4809	0000	0000	0000	0000
0965	4809	0000	0000	0000	0000
0966	5100	0000	0000	0000	0000
0967	2530	0000	0000	0000	0000
0968	4809	0000	0000	0000	0000
0969	4809	0000	0000	0000	0000
096A	0000	0000	0000	0000	0000
096B	4809	0000	0000	0000	0000
096C	0000	0000	0000	0000	0000
096D	4809	0000	0000	0000	0000
096E	4809	0000	0000	0000	0000
096F	2550	0000	0000	0000	0000
0970	6600	0000	0000	0000	0000
0971	4809	0000	0000	0000	0000
0972	5100	0000	0000	0000	0000
0973	5100	0000	0000	0000	0000
0974	2530	0000	0000	0000	0000
0975	4824	0000	0000	0000	0000
0976	1600	0000	0000	0000	0000
0977	4824	0000	0000	0000	0000
0978	3000	0000	0000	0000	0000
0979	6600	0000	0000	0000	0000
097A	5100	0000	0000	0000	0000
097B	2530	0000	0000	0000	0000
097C	4809	0000	0000	0000	0000
097D	2530	0000	0000	0000	0000
097E	4809	0000	0000	0000	0000
097F	2550	0000	0000	0000	0000
097G	6600	0000	0000	0000	0000
0980	5700	0000	0000	0000	0000
0981	4824	0000	0000	0000	0000
0982	7750	0000	0000	0000	0000
0983	5190	0000	0000	0000	0000
0984	4809	0000	0000	0000	0000
0985	1360	0000	0000	0000	0000
0986	4809	0000	0000	0000	0000
0987	4824	0000	0000	0000	0000

```

XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP06F - 1 = AMPCR
STEP
EXEC

OP06F1
OP061 - 1 = MPCR
OP061 - 1 = MPCR
FAULT - 1 = MPCR
OP063 - 1 = MPCR

OP0601
O R = B
Q=SAR, 15=LIT
LIT AND B = B
REGSTACK 1 = CPCR
EINPUT - 1 = CPCR
B = A2
A3 AND LIT = B
15 = LIT
LIT - B = SAR
32 = LIT
B110 C = B
A2 AND B = M1R,B
EOUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

OP0611
LIT AND B = B
15 = LIT
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
LDBLE - 1 = CPCR

LDINX2:
A2 = B
IF LC2 THEN STEP ELSE SKIP %: A1 = IM:
OPCODE - 1 = MPCR
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
LIT + B = M1R
2 = LIT
EOUTPUT - 1 = CPCR
OPCODE - 1 = CPCR

OP063:
RXHFIELD - 1 = CPCR
LDBLE - 1 = CPCR
LDINX2 - 1 = MPCR

OPCODE07:
XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP07F - 1 = AMPCR
STEP
EXEC

```



```

0988 139C 0009 0030 C04C
0989 13CC 0000 0000 C04D
098A 3000 0000 0036 0040
098B 1300 0000 0000 C040

0P07F1
0P070 - 1 = MPCR
0P071 - 1 = MPCR
FAULT - 1 = MPCR
0P073 - 1 = MPCR

0P0701
R R = B
R SARI 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A2
A3 AND LIT = B
15 = LIT
R = SAR
A2 R = A2
IF LET THEN STEP ELSE SKIP X TEST BIT
TEST11 - 1 = MPCR
LIT EOL B
IF TRUE THEN B010 C = B SKIP X SET 00 INTO CC LITS
B011 C = B
B = SAR
A1 AND B = A1
OPCODE - 1 = MPCR

TEST11
LIT EOL B
IF TRUE THEN B010 C = B SKIP X SET 11 IN BOTH LC BITS
B010 C = B
A1 AND B = A1
OPCODE - 1 = MPCR

0P0711
LIT AND B = B
15 = LIT
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A2
B L = BR2
COMP B = SAR
EYULIN - 1 = CPCR
A1 R = A1
16 = SAR
A1 L = A1
A1 OR B = A1
A2 + 1 = A2
A2 L = BR2
COMP B = SAR
EYULIN - 1 = CPCR
B L = MIN
COMP 16 = SAR
LIT L = A3
LIT B
LIT COMP 29 = SAR
LIT B
LIT COMP 16 = SAR
A3 OR B = B

09A5 4809 2C55 0800 00F0
09A6 00F0 00C9 0C70 00E0
09A7 51C0 0000 0C00 00E0
09A8 2F3C 0000 0C70 00E0
09A9 4809 00C0 20C0 00E0
09AA 4809 0C41 001C 00E0
09AB 0000 0000 0C00 00E0
09AC 50E0 0000 0C00 00E0
09AD 4809 00C0 0C00 00E0
09AE 0000 0000 0C00 00E0
09AF 4809 00C1 4C00 00E0
09B0 4809 AC5C 4030 00E0
09B1 4809 00C0 2F00 00E0
09B2 4809 0C00 0C40 00E0
09B3 0000 0C00 0C30 00E0
09B4 50E0 0000 0C30 00E0
09B5 4809 0C41 0C30 00E0
09B6 0000 0C00 0000 00E0
09B7 4809 0000 0C00 00E0
09B8 4809 20C1 4C00 00E0
09B9 4809 20C1 0C30 00E0
09BA 0700 0000 0C30 00E0
09BB 4809 EC5C 0800 00E0

```



```

3 J = LIT
4 = SAR, 15 = LIT
5 B EQU 0
6 IF TRUE THEN SKIP
7 CONTENTERM - 1 = CPCR
8 R L = SAR
9 R L = B
10 16 = SAR
11 A3 OR B = A3
12 IFETCH - 1 = CPCR
13 A3 R = A2
14 A3 R = A2
15 16 = SAR
16 A2 + B = A2
17 A3 R = B
18 A3 R = B
19 4809 E5C0 2030 00F0
20 4809 E0C0 8030 00F0
21 4809 C0C0 6030 00F0
22 4809 25C0 0030 00F0
23 4809 25C0 0030 00F0
24 4809 E5C0 1030 00F0
25 4809 E0C0 8030 00F0
26 4809 25C0 0030 00F0
27 4809 25C0 0030 00F0
28 4809 E5C0 1030 00F0
29 4809 E0C0 8030 00F0
30 4809 25C0 0030 00F0
31 4809 25C0 0030 00F0
32 4809 E5C0 1030 00F0
33 4809 E0C0 8030 00F0
34 4809 25C0 0030 00F0
35 4809 25C0 0030 00F0
36 4809 E5C0 1030 00F0
37 4809 E0C0 8030 00F0
38 4809 25C0 0030 00F0
39 4809 E5C0 1030 00F0
40 4809 E0C0 8030 00F0
41 4809 25C0 0030 00F0
42 4809 25C0 0030 00F0
43 4809 E5C0 1030 00F0
44 4809 E0C0 8030 00F0
45 4809 25C0 0030 00F0
46 4809 E5C0 1030 00F0
47 4809 E0C0 8030 00F0
48 4809 25C0 0030 00F0
49 4809 E5C0 1030 00F0
50 4809 E0C0 8030 00F0
51 4809 25C0 0030 00F0
52 4809 E5C0 1030 00F0
53 4809 E0C0 8030 00F0
54 4809 25C0 0030 00F0
55 4809 E5C0 1030 00F0
56 4809 E0C0 8030 00F0
57 4809 25C0 0030 00F0
58 4809 E5C0 1030 00F0
59 4809 E0C0 8030 00F0
60 4809 25C0 0030 00F0
61 4809 E5C0 1030 00F0
62 4809 E0C0 8030 00F0
63 4809 25C0 0030 00F0
64 4809 E5C0 1030 00F0
65 4809 E0C0 8030 00F0
66 4809 25C0 0030 00F0
67 4809 E5C0 1030 00F0
68 4809 E0C0 8030 00F0
69 4809 25C0 0030 00F0
70 4809 E5C0 1030 00F0
71 4809 E0C0 8030 00F0
72 4809 25C0 0030 00F0
73 4809 E5C0 1030 00F0
74 4809 E0C0 8030 00F0
75 4809 25C0 0030 00F0
76 4809 E5C0 1030 00F0
77 4809 E0C0 8030 00F0
78 4809 25C0 0030 00F0
79 4809 E5C0 1030 00F0
80 4809 E0C0 8030 00F0
81 4809 25C0 0030 00F0
82 4809 E5C0 1030 00F0
83 4809 E0C0 8030 00F0
84 4809 25C0 0030 00F0
85 4809 E5C0 1030 00F0
86 4809 E0C0 8030 00F0
87 4809 25C0 0030 00F0
88 4809 E5C0 1030 00F0
89 4809 E0C0 8030 00F0
90 4809 25C0 0030 00F0
91 4809 E5C0 1030 00F0
92 4809 E0C0 8030 00F0
93 4809 25C0 0030 00F0
94 4809 E5C0 1030 00F0
95 4809 E0C0 8030 00F0
96 4809 25C0 0030 00F0
97 4809 E5C0 1030 00F0
98 4809 E0C0 8030 00F0
99 4809 25C0 0030 00F0
100 4809 E5C0 1030 00F0
101 4809 E0C0 8030 00F0
102 4809 25C0 0030 00F0
103 4809 E5C0 1030 00F0
104 4809 E0C0 8030 00F0
105 4809 25C0 0030 00F0
106 4809 E5C0 1030 00F0
107 4809 E0C0 8030 00F0
108 4809 25C0 0030 00F0
109 4809 E5C0 1030 00F0
110 4809 E0C0 8030 00F0
111 4809 25C0 0030 00F0
112 4809 E5C0 1030 00F0
113 4809 E0C0 8030 00F0
114 4809 25C0 0030 00F0
115 4809 E5C0 1030 00F0
116 4809 E0C0 8030 00F0
117 4809 25C0 0030 00F0
118 4809 E5C0 1030 00F0
119 4809 E0C0 8030 00F0
120 4809 25C0 0030 00F0
121 4809 E5C0 1030 00F0
122 4809 E0C0 8030 00F0
123 4809 25C0 0030 00F0
124 4809 E5C0 1030 00F0
125 4809 E0C0 8030 00F0
126 4809 25C0 0030 00F0
127 4809 E5C0 1030 00F0
128 4809 E0C0 8030 00F0
129 4809 25C0 0030 00F0
130 4809 E5C0 1030 00F0
131 4809 E0C0 8030 00F0
132 4809 25C0 0030 00F0
133 4809 E5C0 1030 00F0
134 4809 E0C0 8030 00F0
135 4809 25C0 0030 00F0
136 4809 E5C0 1030 00F0
137 4809 E0C0 8030 00F0
138 4809 25C0 0030 00F0
139 4809 E5C0 1030 00F0
140 4809 E0C0 8030 00F0
141 4809 25C0 0030 00F0
142 4809 E5C0 1030 00F0
143 4809 E0C0 8030 00F0
144 4809 25C0 0030 00F0
145 4809 E5C0 1030 00F0
146 4809 E0C0 8030 00F0
147 4809 25C0 0030 00F0
148 4809 E5C0 1030 00F0
149 4809 E0C0 8030 00F0
150 4809 25C0 0030 00F0
151 4809 E5C0 1030 00F0
152 4809 E0C0 8030 00F0
153 4809 25C0 0030 00F0
154 4809 E5C0 1030 00F0
155 4809 E0C0 8030 00F0
156 4809 25C0 0030 00F0
157 4809 E5C0 1030 00F0
158 4809 E0C0 8030 00F0
159 4809 25C0 0030 00F0
160 4809 E5C0 1030 00F0
161 4809 E0C0 8030 00F0
162 4809 25C0 0030 00F0
163 4809 E5C0 1030 00F0
164 4809 E0C0 8030 00F0
165 4809 25C0 0030 00F0
166 4809 E5C0 1030 00F0
167 4809 E0C0 8030 00F0
168 4809 25C0 0030 00F0
169 4809 E5C0 1030 00F0
170 4809 E0C0 8030 00F0
171 4809 25C0 0030 00F0
172 4809 E5C0 1030 00F0
173 4809 E0C0 8030 00F0
174 4809 25C0 0030 00F0
175 4809 E5C0 1030 00F0
176 4809 E0C0 8030 00F0
177 4809 25C0 0030 00F0
178 4809 E5C0 1030 00F0
179 4809 E0C0 8030 00F0
180 4809 25C0 0030 00F0
181 4809 E5C0 1030 00F0
182 4809 E0C0 8030 00F0
183 4809 25C0 0030 00F0
184 4809 E5C0 1030 00F0
185 4809 E0C0 8030 00F0
186 4809 25C0 0030 00F0
187 4809 E5C0 1030 00F0
188 4809 E0C0 8030 00F0
189 4809 25C0 0030 00F0
190 4809 E5C0 1030 00F0
191 4809 E0C0 8030 00F0
192
```

OP133:

CPB39	6330	0000	0000	0060
CPB38	3809	0C41	0C00	0C0C
CPB37	0000	0000	0C00	003C
CPB36	3609	E156	2000	00FC
CPB35	80FC	0000	0000	0080
CPB34	3409	E000	9C00	0C0C
CPB33	3309	E155	0B90	00F0
CPB32	4809	CC5E	0B3C	00F0
CPB31	4419	0C46	0600	00F0
CPB2	4809	2C80	0B00	00F0
CPB1	0110	0CC0	0000	00E0
CPB4	4809	0C5F	1D00	00F0
CPB5	000C	0C00	0070	0020


```

0C43 4809 0C5E 0030 80FC      -B = SAR
0C44 4809 C000 9030 C0F0      A2 R = A3
0C45 4809 EC02 0030 C0F0      M01 A3
0C46 53C9 00C0 0030 C0F0      IF NOT APT THEN SET LCL
0C47 4809 0C5E 0030 80FC      00BIT 1 = CPCR
0C48 4809 0C5E 0030 80FC      00BIT 1 = CPCR
0C49 4809 C001 2030 C0F0      A2 L = A2, B1 SET LCL
0C4A 200C 00C0 0030 006C      SETCCA - 1 = CPCR
0C4B 4809 C0C0 0030 20F0      4SR
0C4C 4809 0F43 80C0 C0F0      BHAR R = MAR2
0C4D 000C 00C0 0030 0010      B = SAR
0C4E 48C9 C0C0 8030 C0F0      A2 R = M1R
0C4F 0000 0000 00C0 C020      16 = SAR
0C50 2F30 00C0 C0C0 C060      F0UTPUT - 1 = CPCR
0C51 0010 00C0 0030 00A0      COMP 16 = SAR, 1 = LIT
0C52 4809 C001 2030 C0F0      A2 L = A2
0C53 4809 C0C0 8030 C0F0      A2 R = M1R
0C54 48C9 2FC0 00C0 C0F0      LIT OR BHAR = MAR2
0C55 2F30 00C0 0030 006C      F0UTPUT - 1 = CPCR
0C56 56EC 0003 0030 C040      OPCODE - 1 = MPCR

0P161:
0C57 238C 0000 C030 0060      CONTENTSR - 1 = CPCR
0C58 00C0 00C0 C0C0      C0L = BR1
0C59 002C C0C0 0000 C0F0      COMP 8 = SAR, 2 = LIT
0C5A 4809 2C80 0030 C0F0      BHAR L = BR2
0C5B 51E0 0000 0030 C060      EMULOUT - 1 = CPCR
0C5C 4809 E0C0 8030 C0F0      A3 R = B
0C5D 80FC 0000 0030 0080      LIT AND P = B
0C5E 80FC 0000 0030 0080      15 = LIT, 4 = SAR
0C5F 4809 2C5E 0030 C0F0      REGSTACK - 1 = CPCR
0C60 51C0 0000 0030 C060      A3 = B
0C61 4809 E0C0 C030 C0F0      CONTENTSFA - 1 = CPCR
0C62 228C 00C0 0030 C060      ASR
0C63 4809 0C40 003C C0F0      BHAR + 1 L = BR1
0C64 4809 00C0 007C 20F0      COMP 8 = SAR
0C65 4809 0F43 0010 C0F0      A3 R = MAR2
0C66 61E0 00C0 0030 006C      EMULOUT - 1 = CPCR
0C67 4809 0F43 0030 C030      BHAR + 1 L = BR1
0C68 000C 00C0 0030 C030      COMP 8 = SAR
0C69 4809 E0C0 80C0 C0F0      A3 R = MAR2
0C6A 001C 0000 0000 C0AC      16 = SAR, 1 = LIT
0C6B 4809 2FC0 00C0 C060      LIT OR BHAR = MAR2
0C6C 2F3C 00C0 0030 C060      F0UTPUT - 1 = CPCR
0C6D 4809 0C40 003C C0F0      B = M1R
0C6E 4809 00C0 0030 20F0      BHAR = BR2
0C6F 4809 0F43 0010 C0F0      EMULOUT - 1 = CPCR
0C70 61E0 00C0 0030 C060      OPCODE - 1 = MPCR
0C71 56E0 0000 C030 0040

0P162:
0C72 4809 2C5E 0E3C 00F0      LIT AND B = B
0C73 00FC 0000 0030 00EC      15 = LIT

```



```

0P1711
PCDE 2360 00C3 00D0 0060
0CDF 4809 0C41 0010 00F0
0CE0 0000 0000 0000 0030
0CE1 4809 00C0 0090 00F0
0CE2 61E0 00C0 0090 0060
0CE3 66E0 0000 0000 0040

0P1712
CC04 4809 2C56 00C0 00F0
0CE5 00C0 00C0 0090 00E0
0CE6 4809 0C52 0020 00F0
0CE7 6819 0000 0000 0060
0CE8 236C 0000 0090 00F0
0CE9 4809 0C41 0020 00F0
0CEA 0000 00C0 0090 0020
0CEB 4809 EC5C 1C30 00F0
0CEC 6330 00C0 0000 0060
0CED 4809 ECC0 A000 00F0
0CEE 0000 00C0 0020 0020
0CEF 4809 CC40 2700 00F0
0CF0 4809 ECC0 9000 00F0
0CF1 50F0 00C0 0020 0080
0CF2 4809 E155 0020 00F0
0CF3 51C0 00C0 0090 0060
0CF4 4809 0F41 0C20 00F0
0CF5 001C 0000 00C0 0080
0CF6 2F3C 0000 00C0 0060
0CF7 4809 2F5C 001C 00F0
0CF8 4809 0C41 1C00 00F0
0CF9 0000 00C0 0070 0020
0CEA 2F30 00C0 0020 0060
0CEB 4809 EC5C 3020 00F0
0CEC 4809 C0C3 000C 00F0
0CEE 49C9 E0F1 9B20 00F0
0CFE 2000 00C0 0020 0060
0CF0 4809 E0C1 2C30 00F0
0CF1 0000 00C0 0030 0020
0CF2 4809 C0C0 8030 00F0
0CF3 2F5C 00C0 0020 0060
0CF4 4809 0000 0020 00F0
0CF5 4809 0F43 801C 00F0
0CF6 0000 00C0 0070 0010
0CF7 4809 E000 803C 00F0
0CF8 0000 0000 0000 0020
0CF9 2F50 00C0 0000 0060
0C0A 66E0 00C0 0020 0040

0008 57C0 0000 0020 0060
0C0C 4809 0C41 0010 00F0
0000 0000 00C0 0000 0030
0C0E 4809 0C00 005C 00F0

0P1711
CONTENTSRR - 1 = CPCR
B L = BR2
COMP 6 = SAR
0 = MIR
EOLUT - 1 = CPCR
OPCODE - 1 = HPCR

LIT AND B = B
15 = LIT
C EOL B
IF TRUE THEN SKIP
CONTENTSRR - 1 = CPCR
B L = B
COMP 16 = SAR
A3 OR D = A3
IFETCH - 1 = CPCR
A3 R = A2
16 = SAR
A2 + B = A2
A3 R = A3
A4 = SAR; 15 = LIT
A3 AND LIT = B
REGSTACK - 1 = CPCR
BHAR L = BR1
COMP 8 = SAR; 1 = LIT
EINP - 1 = CPCR
LIT OR BHAR = HAR2
P L = A3
COMP 16 = SAR
EINP - 1 = CPCR
A3 OR B = A3
A2 = A2
A3 R = SAR
A3 C = A3; 81 SET LC1
SETCCA - 1 = CPCR
A3 L = A2
COMP 16 = SAR
A2 R = MIR
EOUTP - 1 = CPCR
ASR
BHAR R = HAR2
R = SAR
A3 R = MIR
16 = SAR
EOUTP - 1 = CPCR
OPCODE - 1 = HPCR

RXHFIEL0 - 1 = CPCR
B L = BR2
COMP 8 = SAR
C = MIR

0P173:
RXHFIEL0 - 1 = CPCR
B L = BR2
COMP 8 = SAR
C = MIR

```


[illegible]


```

0031 0000 0000 0000 0000
0032 0000 0000 0000 0000
0033 4809 0000 0000 0000
0034 2F50 0000 0000 0000
0035 0000 0000 0000 0000
0036 0000 0000 0000 0000
0037 0000 0000 0000 0000
0038 0000 0000 0000 0000
0039 0000 0000 0000 0000
0040 0000 0000 0000 0000
0041 0000 0000 0000 0000
0042 0000 0000 0000 0000

```

002021

```

0043 4809 2055 0000 0000
0044 0000 0000 0000 0000
0045 4809 0052 0000 0000
0046 6819 0000 0000 0000
0047 236C 0000 0000 0000
0048 4809 0041 0000 0000
0049 0000 0000 0000 0000
0050 0000 0000 0000 0000
0051 4809 0052 0000 0000
0052 4809 0000 0000 0000
0053 4809 0000 0000 0000
0054 4809 0000 0000 0000
0055 4809 0000 0000 0000
0056 4809 0000 0000 0000
0057 4809 0000 0000 0000
0058 4809 0000 0000 0000
0059 4809 0000 0000 0000
0060 4809 0000 0000 0000
0061 4809 0000 0000 0000
0062 4809 0000 0000 0000
0063 4809 0000 0000 0000
0064 4809 0000 0000 0000
0065 4809 0000 0000 0000
0066 4809 0000 0000 0000
0067 4809 0000 0000 0000
0068 4809 0000 0000 0000
0069 4809 0000 0000 0000
0070 4809 0000 0000 0000
0071 4809 0000 0000 0000
0072 4809 0000 0000 0000
0073 4809 0000 0000 0000
0074 4809 0000 0000 0000
0075 4809 0000 0000 0000
0076 4809 0000 0000 0000
0077 4809 0000 0000 0000
0078 4809 0000 0000 0000
0079 4809 0000 0000 0000
0080 4809 0000 0000 0000
0081 4809 0000 0000 0000
0082 4809 0000 0000 0000
0083 4809 0000 0000 0000
0084 4809 0000 0000 0000
0085 4809 0000 0000 0000
0086 4809 0000 0000 0000
0087 4809 0000 0000 0000
0088 4809 0000 0000 0000
0089 4809 0000 0000 0000
0090 4809 0000 0000 0000
0091 4809 0000 0000 0000
0092 4809 0000 0000 0000
0093 4809 0000 0000 0000
0094 4809 0000 0000 0000
0095 4809 0000 0000 0000
0096 4809 0000 0000 0000
0097 4809 0000 0000 0000
0098 4809 0000 0000 0000
0099 4809 0000 0000 0000
0100 4809 0000 0000 0000

```

002031

```

0050 5700 0000 0000 0000
0051 0000 0000 0000 0000
0052 0000 0000 0000 0000
0053 0000 0000 0000 0000
0054 0000 0000 0000 0000
0055 0000 0000 0000 0000
0056 0000 0000 0000 0000
0057 0000 0000 0000 0000
0058 0000 0000 0000 0000
0059 0000 0000 0000 0000
0060 0000 0000 0000 0000
0061 0000 0000 0000 0000
0062 0000 0000 0000 0000
0063 0000 0000 0000 0000
0064 0000 0000 0000 0000
0065 0000 0000 0000 0000
0066 0000 0000 0000 0000
0067 0000 0000 0000 0000
0068 0000 0000 0000 0000
0069 0000 0000 0000 0000
0070 0000 0000 0000 0000
0071 0000 0000 0000 0000
0072 0000 0000 0000 0000
0073 0000 0000 0000 0000
0074 0000 0000 0000 0000
0075 0000 0000 0000 0000
0076 0000 0000 0000 0000
0077 0000 0000 0000 0000
0078 0000 0000 0000 0000
0079 0000 0000 0000 0000
0080 0000 0000 0000 0000
0081 0000 0000 0000 0000
0082 0000 0000 0000 0000
0083 0000 0000 0000 0000
0084 0000 0000 0000 0000
0085 0000 0000 0000 0000
0086 0000 0000 0000 0000
0087 0000 0000 0000 0000
0088 0000 0000 0000 0000
0089 0000 0000 0000 0000
0090 0000 0000 0000 0000
0091 0000 0000 0000 0000
0092 0000 0000 0000 0000
0093 0000 0000 0000 0000
0094 0000 0000 0000 0000
0095 0000 0000 0000 0000
0096 0000 0000 0000 0000
0097 0000 0000 0000 0000
0098 0000 0000 0000 0000
0099 0000 0000 0000 0000
0100 0000 0000 0000 0000

```



```

0071 3690 0000 0000 0060
0072 0000 0000 0000 0000
0073 4800 0000 0000 0000
0074 4800 0000 0000 0000
0075 4824 0000 0000 0000

0076 16FC 0000 0000 0000
0077 1700 0000 0000 0000
0078 3000 0000 0000 0000
0079 1710 0000 0000 0000

007A 4809 0000 0000 0000
007B 30F0 0000 0000 0000
007C 4809 2C50 0000 0000
007D 51CC 0000 0000 0000
007E 2F30 0000 0000 0000
007F 4809 0041 2030 0000
0080 0000 0000 0000 0000
0081 4809 0041 0030 0000
0082 001C 0000 0000 0000
0083 4809 2F50 0000 0000
0084 4809 0000 0000 0000
0085 4809 CC50 0000 0000
0086 4809 E150 0000 0000
0087 0000 0000 0000 0000
0088 51C0 0000 0000 0000
0089 2F30 0000 0000 0000
0090 0010 0000 0000 0000
0091 4809 2F50 0000 0000
0092 2F30 0000 0000 0000
0093 4809 CC50 0000 0000
0094 78C9 0000 0000 0000
0095 4F10 0000 0000 0000
0096 49C9 0000 0000 0000
0097 2000 0000 0000 0000
0098 4809 0000 0000 0000
0099 4809 0040 0030 0000
009A 5000 0000 0000 0000
009B 4809 CC41 0000 0000
009C 4809 0000 0000 0000
009D 4809 0000 0000 0000
009E 4809 0000 0000 0000
009F 4809 0000 0000 0000
00A0 2F50 0000 0000 0000
00A1 56EC 0000 0000 0000

00C00E21: XFCODE - 1 = CPCR
           A2 = AMPCR = AMPCR
           021F - 1 = AMPCR
           SIEP
           EXEC

0P21F:
           0P210 - 1 = MPCR
           0P211 - 1 = MPCR
           FAULT - 1 = MPCR
           0P213 - 1 = MPCR

           B R = B
           4 = SARI 15 = LIT
           LIT AND 0 = 0
           REGSTACK - 1 = CPCR
           EQUIPUT - 1 = CPCR
           B L = A2
           COMP 16 = SAR
           BHAR L = BRI
           COMP 8 = SARI 1 = LIT
           LIT OR BHAR = MAR2
           EQUIPUT - 1 = CPCR
           A2 OR 0 = A2
           A2 AND LIT = B
           15 = LIT
           REGSTACK - 1 = CPCR
           EQUIPUT - 1 = CPCR
           B L = A3
           COMP 16 = SARI 1 = LIT
           LIT OR BHAR = MAR2
           EQUIPUT - 1 = CPCR
           A3 OR B = B
           A2 - 0 = MIR; SET LC2
           IF A0V THEN SET LC1
           CARRY - 1 = CPCR
           CHECKOV - 1 = CPCR
           BHIF SET LC1
           SETCCA - 1 = CPCR
           BHI
           B R = MIR
           16 = SAR
           B L = B
           B R = B
           BHAR R = MAR2, A3
           EQUIPUT - 1 = CPCR
           A3 OR 1 = MAR2
           B = MIR
           EQUIPUT - 1 = CPCR
           0PCODE - 1 = MPCR

0P210:
           0P211:
           0P212:
           0P213:
           0P214:
           0P215:
           0P216:
           0P217:
           0P218:
           0P219:
           0P21A:
           0P21B:
           0P21C:
           0P21D:
           0P21E:
           0P21F:
           0P21G:
           0P21H:
           0P21I:
           0P21J:
           0P21K:
           0P21L:
           0P21M:
           0P21N:
           0P21O:
           0P21P:
           0P21Q:
           0P21R:
           0P21S:
           0P21T:
           0P21U:
           0P21V:
           0P21W:
           0P21X:
           0P21Y:
           0P21Z:
           0P21AA:
           0P21AB:
           0P21AC:
           0P21AD:
           0P21AE:
           0P21AF:
           0P21AG:
           0P21AH:
           0P21AI:
           0P21AJ:
           0P21AK:
           0P21AL:
           0P21AM:
           0P21AN:
           0P21AO:
           0P21AP:
           0P21AQ:
           0P21AR:
           0P21AS:
           0P21AT:
           0P21AU:
           0P21AV:
           0P21AW:
           0P21AX:
           0P21AY:
           0P21AZ:
           0P21BA:
           0P21BB:
           0P21BC:
           0P21BD:
           0P21BE:
           0P21BF:
           0P21BG:
           0P21BH:
           0P21BI:
           0P21BJ:
           0P21BK:
           0P21BL:
           0P21BM:
           0P21BN:
           0P21BO:
           0P21BP:
           0P21BQ:
           0P21BR:
           0P21BS:
           0P21BT:
           0P21BU:
           0P21BV:
           0P21BW:
           0P21BX:
           0P21BY:
           0P21BZ:
           0P21CA:
           0P21CB:
           0P21CC:
           0P21CD:
           0P21CE:
           0P21CF:
           0P21CG:
           0P21CH:
           0P21CI:
           0P21CJ:
           0P21CK:
           0P21CL:
           0P21CM:
           0P21CN:
           0P21CO:
           0P21CP:
           0P21CQ:
           0P21CR:
           0P21CS:
           0P21CT:
           0P21CU:
           0P21CV:
           0P21CW:
           0P21CX:
           0P21CY:
           0P21CZ:
           0P21DA:
           0P21DB:
           0P21DC:
           0P21DD:
           0P21DE:
           0P21DF:
           0P21DG:
           0P21DH:
           0P21DI:
           0P21DJ:
           0P21DK:
           0P21DL:
           0P21DM:
           0P21DN:
           0P21DO:
           0P21DP:
           0P21DQ:
           0P21DR:
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           0P21ZR:
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           0P21ZT:
           0P21ZU:
           0P21ZV:
           0P21ZW:
           0P21ZX:
           0P21ZY:
           0P21ZZ

```


047236500 0
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047237500 0
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047290000 0
047291000 0
047292000 0
047293000 0
047294000 0
047295000 0
047296000 0
047297000 0
047298000 0
047299000 0


```

0F3E 51CC 00C0 00D0 0060 REGSTACK - 1 = CPCR
0F3F 2F3C 00C0 0070 0060 INPUT - 1 = CPCR
0F40 4809 0C41 1C30 00F0 P L = A3
0F41 001C 00C0 0070 00A0 COMP 16 = SAR J = LIT
0F42 4809 2F3C 001C 00F0 LIT OR BHAR = MAR2
0F43 2F3C 00C0 0070 0060 INPUT - 1 = CPCR
0F44 4809 1C30 0070 0060 A3 OR B = E, MIR
0F45 20CC 00C0 0070 0060 SETCC - 1 = CPCR
0F46 4809 00C0 0070 00F0 EMI - B = MIR, SET LC2
0F47 4809 00C0 0070 00F0 A2 - A0V THEN SET CL
0F48 70C5 00C0 0070 00F0 CARRY - 1 = CPCR
0F49 1E7C 00C0 0070 0060 CHECKOV - 1 = CPCR
0F4A 9F1C 00C0 0070 0060 OPCODE - 1 = MPCC
0F4B 66FC 00C0 0070 00A0

0F4C 4809 0C40 803C 00F0 B R = R
0F4D 30FC 00C0 0070 0060 4 = SAR J 15 = LIT
0F4E 4809 2C56 C0D0 C0F0 LIT AND B = E
0F4F 31CC 00C0 0070 C0F0 REGSTACK - 1 = CPCR
0F50 2F3C 00C0 0070 C060 INPUT - 1 = CPCR
0F51 4809 0C41 20C0 00F0 B L = A2
0F52 3010 00C0 C0D0 00A0 COMP 16 = SAR J 1 = LIT
0F53 4809 2F3C 001C 00F0 LIT OR DHAR = MAR2
0F54 2F3C 00C0 0070 0060 INPUT - 1 = CPCR
0F55 4809 C05C 2070 00F0 A2 OR B = A2
0F56 4809 E156 C03C 00F0 A3 AND LIT = B
0F57 30F0 00C0 0070 0060 15 = LIT
0F58 31CC 00C0 0070 0060 REGSTACK - 1 = CPCR
0F59 4809 0C41 0C10 00F0 BHAR L = BHAR
0F5A 30CC 00C0 0070 003C COMP B = SAR
0F5B 50E0 00C0 0070 0060 ENULIN - 1 = CPCR
0F5C 00C0 0070 1C30 00F0 B L = A3
0F5D 4809 0C41 20C0 00F0 LIT OR BHAR L = MAR2
0F5E 4809 2F3C 001C 00F0 COMP B SAR
0F5F 30C0 00C0 0070 C03C ENULIN - 1 = CPCR
0F60 60E0 00C0 0070 C020 A3 OR B = B, MIR
0F61 4809 EC57 0030 00F0 SETCC - 1 = CPCR
0F62 20CC 00C0 0070 C0F0 EMI
0F63 4809 00C0 0070 C0F0 A2 - B = MIR, SET LC2
0F64 4849 CC5E 00C0 C060 IF A0V THEN SET LC1
0F65 7BC9 00C0 0070 C0F0 CARRY - 1 = CPCR
0F66 1E7C C0D0 0070 C060 CHECKOV - 1 = CPCR
0F67 4F1C 00C0 0070 C060 OPCODE - 1 = MPCC
0F68 66E0 00C0 C0C0 C0A0

0F69 5700 00C0 0070 0060 RMFIELD - 1 = CPCR
0F6A 4809 0C41 0C1C 00F0 D L = ER2
0F6B 00CC 00C0 0070 C030 COMP B = SAR
0F6C 4809 00C0 0070 C030 ENULIN - 1 = CPCR
0F6D 4805 CC40 0070 C060 LIT OR BHAR L = MAR2
0F6E 0010 00C0 0070 00A0 COMP 16 = SAR J 1 = LIT
0F6F 4809 2F3C 001C C0F0 LIT OR BHAR L = ER2

```

0F251:

```

X R1 TYPE 2 COMPARE DOUBBLE
X (R(A),R(A+1)):(Y,Y+1)
X SET CC, CARRY, AND OV BITS

```

```

B R = R
4 = SAR J 15 = LIT
LIT AND B = E
REGSTACK - 1 = CPCR
INPUT - 1 = CPCR
B L = A2
COMP 16 = SAR J 1 = LIT
LIT OR DHAR = MAR2
INPUT - 1 = CPCR
A2 OR B = A2
A3 AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
BHAR L = BHAR
COMP B = SAR
ENULIN - 1 = CPCR
B L = A3
LIT OR BHAR L = MAR2
COMP B SAR
ENULIN - 1 = CPCR
A3 OR B = B, MIR
SETCC - 1 = CPCR
EMI
A2 - B = MIR, SET LC2
IF A0V THEN SET LC1
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
OPCODE - 1 = MPCC

```

```

X ISOLATE *A* FIELD
X (R(A)) INTO B
X (R(A)) INTO HS WORD OF A2
X (R(A+1))
X (R(A+1)) INTO B
X A2 = (R(A))/(R(A+1))
X ISOLATE *M* FIELD
X (R(A),R(A+1)):(Y,Y+1)
X SET CC, CARRY, AND OV BITS

```

```

X (Y*) INTO B
X (Y*) INTO HS WORD OF A3
X (Y*) INTO B
X ADDR OF Y* + 1
X (Y*) INTO B
X B = (Y*)/(Y*+1)
X SET THE CONDITION BITS

```

```

X TYPE RX DOUBLE COMPARE
X (R(A),R(A+1)):(Y,Y+1)
X SET CC, CARRY AND OV BITS
X Y INTO F

```

```

X (Y) INTO B
X (Y) INTO HS WORD OF A2
LIT OR BHAR L = ER2
X ADDR OF Y+1

```

0F253:

```

X TYPE RX DOUBLE COMPARE
X (R(A),R(A+1)):(Y,Y+1)
X SET CC, CARRY AND OV BITS
X Y INTO F

```

```

X (Y) INTO B
X (Y) INTO HS WORD OF A2
LIT OR BHAR L = ER2
X ADDR OF Y+1

```


OP070	0600 0000 00C0 00A0	COMP 0 = SAR	% (Y+1) INTO B	05094000 0
OP071	60E0 0000 0000 00E0	EYULIN - 1 = CPCR	% MIR = (Y)/(Y+1)	05099600 0
OP072	4809 C0C0 0000 00F0	A3 OR B = MIR		05101000 0
OP073	4809 C0C0 9000 C0F0	A3 R = A3		05101000 0
OP074	50F0 0000 0000 C0E0	A = SAR, I5 = LIT		05102000 0
OP075	4839 E1E0 0000 C0F0	A3 AND LIT = 0	% ISOLATE *A*	05103000 0
OP076	51C0 0000 0000 C0E0	REGSTACK - 1 = CPCR	% (R(A)) INTO E	05104000 0
OP077	2F30 0000 0000 C0E0	EINPUT - 1 = CPCR	% (R(A)) INTO I5 WORD 0F A2	05105000 0
OP078	4809 0041 2000 00F0	R 1 = A2	% (R(A)) INTO I5	05106000 0
OP079	001C 0000 0000 C0A0	COMP 16 = SAR, I = LIT	% (R(A+1))	05107000 0
OP07A	4809 21E0 C01C 00F0	LIT OR BHAR = MAR2	% (R(A+1)) INTO B	05108000 0
OP07B	2E50 0000 0000 C0E0	EINPUT - 1 = CPCR	% A2 = (R(A))/(R(A+1))	05109000 0
OP07C	2000 0000 0000 C0E0	E2 OR B = A2, DM1	% SET THE CONDITION BITS	05110000 0
OP07D	2000 0000 0000 C0E0	SE1CC - 1 = CPCR		05111000 0
OP07E	4809 C0C0 0000 001C	DM1		05112000 0
OP07F	4849 C0E0 C000 00F0	DM1 D = MIR, SET LC2		05113000 0
OP080	7809 0000 0000 C000	IF AND THEN SET LC1		05114000 0
OP08A	1E7C 0000 0000 C000	CARRY - 1 = CPCR		05115000 0
OP08B	4E1C 00C0 0000 C0E0	CHECKOV - 1 = CPCR		05116000 0
OP08C	66E0 C000 0000 C0A0	OPCODE - 1 = NPCC		05117000 0
OP08D	5F9C 0000 0000 00A0	OPCODE261		05118000 0
OP08E	4809 C640 C040 00F0	YFCODE - 1 = CPCR	% I*F INTO A2	05119000 0
OP08F	0186 184C 00C0 C000 C0C0	A2 + AMPCR = AMPCR		05120000 0
OP08G	0186 184C 00C0 C000 C0C0	OP26F - 1 = AMPCR		05121000 0
OP08H	4809 C0C0 0000 00F0	STEP		05122000 0
OP08I	4824 0000 0000 C0F0	EXEC		05123000 0
OP08J	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05124000 0
OP08K	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05125000 0
OP08L	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05126000 0
OP08M	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05127000 0
OP08N	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05128000 0
OP08O	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05129000 0
OP08P	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05130000 0
OP08Q	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05131000 0
OP08R	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05132000 0
OP08S	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05133000 0
OP08T	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05134000 0
OP08U	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05135000 0
OP08V	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05136000 0
OP08W	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05137000 0
OP08X	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05138000 0
OP08Y	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05139000 0
OP08Z	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05140000 0
OP08A	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05141000 0
OP08B	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05142000 0
OP08C	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05143000 0
OP08D	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05144000 0
OP08E	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05145000 0
OP08F	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05146000 0
OP08G	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05147000 0
OP08H	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05148000 0
OP08I	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05149000 0
OP08J	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		05150000 0
OP08K	1880 0000 0000 C0A0	OP263 - 1 = HPCR		05151000 0
OP08L	1850 C0C0 00C0 00A0	OP260 - 1 = HPCR		05152000 0
OP08M	1860 C0C0 0000 C0A0	OP261 - 1 = HPCR		05153000 0
OP08N	187C 00C0 0000 C0A0	OP262 - 1 = HPCR		


```

0FA5 51CC 0000 0000 0000
0FA6 4809 EC01 403C 00F0
0FA7 0000 0000 0000 0000
0FA8 0000 0000 0000 0000
0FA9 2F50 0000 0000 0000
0FAA 56E0 0000 0000 0000

0P2611
CFAC 4809 CC40 880C 00F0
CFAC 3CFC 0000 0000 0000
CFAD 4809 2C55 680C 00F0
0FAE 51CC 0000 0000 0000
0FAF 4809 0F41 007C 00F0
0FB0 0000 0000 0000 0000
0FB1 4809 0F46 003C 00F0
0FB2 51CC 0000 0000 0000
0FB3 2F30 0000 0000 0000
0FB4 4809 0000 203C 00F0
0FB5 4809 1156 0000 00F0
0FB6 0000 0000 0000 0000
0FB7 51CC 0000 0000 0000
0FB8 2F30 0000 0000 0000
0FB9 4809 0C41 0040 00F0
0FBA 0000 0000 0000 0000
0FBC 51CC 0000 0000 0000
0FBD 4809 0000 0000 0000
0FBE 2000 0000 0000 0000
0FBF 4809 0000 803C 00F0
0FC0 0000 0000 0000 0000
0FC1 4809 0000 0000 20F0
0FC2 4809 0F47 801C 00F0
0FC3 0000 0000 0000 0000
0FC4 2F50 0000 0000 0000
0FC5 4809 0F45 0000 0000
0FC6 51CC 0000 0000 0000
0FC7 4809 E001 1000 00F0
0FC8 0000 0000 0000 0000
0FC9 4809 E000 803C 00F0
0FCA 2F50 0000 0000 0000
0FCB 66E0 0000 0000 0000

0P2621
CFCC 4809 2C55 680C 00F0
CFCD 4809 0000 0000 0000
CFCE 4809 0000 0000 0000
CFCF 5810 0000 0000 0000
0F00 238C 0000 0000 0000
CF01 4809 0C41 0030 00F0
CF02 0000 0000 0000 0000
CF03 4809 EC5E 107C 00F0
CF04 4330 0000 0000 0000
0F05 4809 E000 4000 00F0
0F06 0000 0000 0000 0000
CF07 4809 CC40 2C30 00F0
CF08 4809 E000 8800 00F0

REGSTACK - 1 = CPCR
A3 L = A3
COMP 16 = SAR
A3 OUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

R R = P
LIT AND B = B
REGSTACK - 1 = CPCR
B MAR L = B#1
COMP 8 = SAR
B MAR + 1 = B
REGSTACK - 1 = CPCR
INPUT - 1 = CPCR
B = A2
A3 AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
INPUT - 1 = CPCR
F L = B#2
COMP 8 = SAR
F MULIN - 1 = CPCR
MULT - 1 = CPCR
A3 ECCA - 1 = CPCR
A3 R = MIR
16 = SAR
ASR
B MAR R = MAR2
B = SAR
EUIPUT - 1 = CPCR
B MAR + 1 = B
REGSTACK - 1 = CPCR
A3 L = A3
COMP 16 = SAR
A3 R = MIR
EUIPUT - 1 = CPCR
OPCODE - 1 = MPCR

% DI TYPE 2 MULTIPLY (INDIRECT), SET CC
% (RCA+1) X (Y*) = R(A),R(A+1), SET CC
% ISOLATE *A*
% R(A)
% R(A+1)
% (R(A+1)) INTO MAR2
% (RCA+1) INTO B
% (RCA+1) INTO A2
% ISOLATE *M*
% (R(M)) INTO MAR2
% Y* INTO E
% (Y*) INTO B
% MULTI (RCA+1) X (Y*)
% PRODUCT IN A3
% SET THE CONDITION BITS
% (R(A))
% DEF ERI
% R(A)
% R(A+1)
% (R(A+1)) INTO MAR2
% TYPE RK MULTIPLY (CONSTANT)
% (RCA+1) X Y = R(A),R(A+1), SET CC
% ISOLATE *M*
% CHECK FOR H = 0
% (R(R)) INTO B
% A3 = (R(M))/INSTRUCTION
% Y* INTO B
% (R(M)) INTO A2
% Y INTO B

```


[illegible][illegible]

OP263:

5700	00FEF1	00FEF2	00FEF3	00FEF4	00FEF5	00FEF6	00FEF7	00FEF8	00FEF9	00FEFA	00FEFB	00FEFC	00FEFD	00FEFE	00FEFF	00FF00	00FF01	00FF02	00FF03	00FF04	00FF05	00FF06	00FF07	00FF08	00FF09	00FF0A	00FF0B	00FF0C	00FF0D	00FF0E	00FF0F	00FF10	00FF11	00FF12	00FF13	00FF14	00FF15	00FF16	00FF17	00FF18	00FF19	00FF1A	00FF1B	00FF1C	00FF1D	00FF1E	00FF1F	00FF20	00FF21	00FF22	00FF23	00FF24	00FF25	00FF26	00FF27	00FF28	00FF29	00FF2A	00FF2B	00FF2C	00FF2D	00FF2E	00FF2F	00FF30	00FF31	00FF32	00FF33	00FF34	00FF35	00FF36	00FF37	00FF38	00FF39	00FF3A	00FF3B	00FF3C	00FF3D	00FF3E	00FF3F	00FF40	00FF41	00FF42	00FF43	00FF44	00FF45	00FF46	00FF47	00FF48	00FF49	00FF4A	00FF4B	00FF4C	00FF4D	00FF4E	00FF4F	00FF50	00FF51	00FF52	00FF53	00FF54	00FF55	00FF56	00FF57	00FF58	00FF59	00FF5A	00FF5B	00FF5C	00FF5D	00FF5E	00FF5F	00FF60	00FF61	00FF62	00FF63	00FF64	00FF65	00FF66	00FF67	00FF68	00FF69	00FF6A	00FF6B	00FF6C	00FF6D	00FF6E	00FF6F	00FF70	00FF71	00FF72	00FF73	00FF74	00FF75	00FF76	00FF77	00FF78	00FF79	00FF7A	00FF7B	00FF7C	00FF7D	00FF7E	00FF7F	00FF80	00FF81	00FF82	00FF83	00FF84	00FF85	00FF86	00FF87	00FF88	00FF89	00FF8A	00FF8B	00FF8C	00FF8D	00FF8E	00FF8F	00FF90	00FF91	00FF92	00FF93	00FF94	00FF95	00FF96	00FF97	00FF98	00FF99	00FF9A	00FF9B	00FF9C	00FF9D	00FF9E	00FF9F	00FFA0	00FFA1	00FFA2	00FFA3	00FFA4	00FFA5	00FFA6	00FFA7	00FFA8	00FFA9	00FFAA	00FFAB	00FFAC	00FFAD	00FFAE	00FFAF	00FFB0	00FFB1	00FFB2	00FFB3	00FFB4	00FFB5	00FFB6	00FFB7	00FFB8	00FFB9	00FFBA	00FFBB	00FFBC	00FFBD	00FFBE	00FFBF	00FFC0	00FFC1	00FFC2	00FFC3	00FFC4	00FFC5	00FFC6	00FFC7	00FFC8	00FFC9	00FFCA	00FFCB	00FFCC	00FFCD	00FFCE	00FFCF	00FFD0	00FFD1	00FFD2	00FFD3	00FFD4	00FFD5	00FFD6	00FFD7	00FFD8	00FFD9	00FFDA	00FFDB	00FFDC	00FFDD	00FFDE	00FFDF	00FFE0	00FFE1	00FFE2	00FFE3	00FFE4	00FFE5	00FFE6	00FFE7	00FFE8	00FFE9	00FFEA	00FFEB	00FFEC	00FFED	00FFEE	00FFEF	00FFF0	00FFF1	00FFF2	00FFF3	00FFF4	00FFF5	00FFF6	00FFF7	00FFF8	00FFF9	00FFFA	00FFFB	00FFFC	00FFFD	00FFFE	00FFFF	000000	000001	000002	000003	000004	000005	000006	000007	000008	000009	00000A	00000B	00000C	00000D	00000E	00000F	000010	000011	000012	000013	000014	000015	000016	000017	000018	000019	00001A	00001B	00001C	00001D	00001E	00001F	000020	000021	000022	000023	000024	000025	000026	000027	000028	000029	00002A	00002B	00002C	00002D	00002E	00002F	000030	000031	000032	000033	000034	000035	000036	000037	000038	000039	00003A	00003B	00003C	00003D	00003E	00003F	000040	000041	000042	000043	000044	000045	000046	000047	000048	000049	00004A	00004B	00004C	00004D	00004E	00004F	000050	000051	000052	000053	000054	000055	000056	000057	000058	000059	00005A	00005B	00005C	00005D	00005E	00005F	000060	000061	000062	000063	000064	000065	000066	000067	000068	000069	00006A	00006B	00006C	00006D	00006E	00006F	000070	000071	000072	000073	000074	000075	000076	000077	000078	000079	00007A	00007B	00007C	00007D	00007E	00007F	00
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```

X(RX TYPE, MULTIPLY, R(R(A+1))) X (Y)
X(R(A), R(A+1)), AND SET CC
Y INTO 0

X (Y) INTO 0

X ISOLATE "A"
X SAVE R(A)

X(R(A+1))
X(R(A+1)) INTO HAR2
X(R(A+1)) INTO 0

X MULTIPLY R(R(A+1)) X (Y)
X PRODUCT IN A3
X SET THE CONDITION BITS
X(R(A))

REF PR1
X(R(A))

X(R(A+1))
X(R(A+1)) INTO PAR2

```

0	301.6250	0	301.6250
1	302.1250	0	302.1250
2	302.6250	0	302.6250
3	303.1250	0	303.1250
4	303.6250	0	303.6250
5	304.1250	0	304.1250
6	304.6250	0	304.6250
7	305.1250	0	305.1250
8	305.6250	0	305.6250
9	306.1250	0	306.1250
10	306.6250	0	306.6250
11	307.1250	0	307.1250
12	307.6250	0	307.6250
13	308.1250	0	308.1250
14	308.6250	0	308.6250
15	309.1250	0	309.1250
16	309.6250	0	309.6250
17	310.1250	0	310.1250
18	310.6250	0	310.6250
19	311.1250	0	311.1250
20	311.6250	0	311.6250
21	312.1250	0	312.1250
22	312.6250	0	312.6250
23	313.1250	0	313.1250
24	313.6250	0	313.6250
25	314.1250	0	314.1250
26	314.6250	0	314.6250
27	315.1250	0	315.1250
28	315.6250	0	315.6250
29	316.1250	0	316.1250
30	316.6250	0	316.6250
31	317.1250	0	317.1250
32	317.6250	0	317.6250
33	318.1250	0	318.1250
34	318.6250	0	318.6250
35	319.1250	0	319.1250
36	319.6250	0	319.6250
37	320.1250	0	320.1250
38	320.6250	0	320.6250
39	321.1250	0	321.1250
40	321.6250	0	321.6250
41	322.1250	0	322.1250
42	322.6250	0	322.6250
43	323.1250	0	323.1250
44	323.6250	0	323.6250
45	324.1250	0	324.1250
46	324.6250	0	324.6250
47	325.1250	0	325.1250
48	325.6250	0	325.6250
49	326.1250	0	326.1250
50	326.6250	0	326.6250
51	327.1250	0	327.1250
52	327.6250	0	327.6250
53	328.1250	0	328.1250
54	328.6250	0	328.6250
55	329.1250	0	329.1250
56	329.6250	0	329.6250
57	330.1250	0	330.1250
58	330.6250	0	330.6250
59	331.1250	0	331.1250
60	331.6250	0	331.6250
61	332.1250	0	332.1250
62	332.6250	0	332.6250
63	333.1250	0	333.1250
64	333.6250	0	333.6250
65	334.1250	0	334.1250
66	334.6250	0	334.6250
67	335.1250	0	335.1250
68	335.6250	0	335.6250
69	336.1250	0	336.1250
70	336.6250	0	336.6250
71	337.1250	0	337.1250
72	337.6250	0	337.6250
73	338.1250	0	338.1250
74	338.6250	0	338.6250
75	339.1250	0	339.1250
76	339.6250	0	339.6250
77	340.1250	0	340.1250
78	340.6250	0	340.6250
79	341.1250	0	341.1250
80	341.6250	0	341.6250
81	342.1250	0	342.1250
82	342.6250	0	342.6250
83	343.1250	0	343.1250
84	343.6250	0	343.6250
85	344.1250	0	344.1250
86	344.6250	0	344.6250
87	345.1250	0	345.1250
88	345.6250	0	345.6250
89	346.1250	0	346.1250
90	346.6250	0	346.6250
91	347.1250	0	347.1250
92	347.6250	0	347.6250
9			


```

1C40 31C0 00E9 C070 00E6 02338C0C D
1C41 48C9 CF41 0020 C0F0 05339000 C
1C42 48C9 CF41 0020 C0F0 05340000 C
1C43 2F3C 00C2 00C0 00C0 05341000 D
1C44 4809 0C41 25C0 00C0 05342000 D
1C45 00C0 0000 00C0 00C0 05343000 D
1C46 4809 0F46 0020 00F0 05344000 D
1C47 31C0 00C2 00C0 00C0 05345000 D
1C48 2F3C 00C0 00C0 00C0 05346000 D
1C49 4809 C05C 25C0 00F0 05347000 D
1C4A 4809 E156 00C0 00F0 05348000 D
1C4B 00F0 C0C0 00C0 00C0 05349000 D
1C4C 31C0 C0C0 00C0 00C0 0534A000 D
1C4D 2F3C 00C0 00C0 00C0 0534B000 D
1C4E 4809 0C41 001C 00C0 0534C000 D
1C4F 0000 00C0 00C0 00C0 0534D000 D
1C50 50E0 00C0 00C0 00C0 0534E000 D
1C51 48C9 0C41 08C0 00C0 0534F000 D
1C52 2000 00C0 00C0 00C0 05350000 D
1C53 2000 00C0 00C0 00C0 05351000 D
1C54 20B0 C0C0 00C0 00C0 05352000 D
1C55 50AC 00C0 00C0 00C0 05353000 D
1C56 2819 00C0 00C0 00C0 05354000 D
1C57 5050 00C0 00C0 00C0 05355000 D
1C58 4809 C0C0 00C0 00C0 05356000 D
1C59 2000 00C0 00C0 00C0 05357000 D
1C5A 2000 00C0 00C0 00C0 05358000 D
1C5B 4809 0C20 00C0 20FC 05359000 D
1C5C 4809 0F42 851C 00F0 05360000 D
1C5D 3000 C0C0 00C0 00C0 05361000 D
1C5E 2F5F 00C0 00C0 00C0 05362000 D
1C5F 4809 E0C3 00C0 00C0 05363000 D
1C60 48C9 0F46 0830 00F0 05364000 D
1C61 51C0 C0C0 00C0 00C0 05365000 D
1C62 2F5C C0C0 00C0 00C0 05366000 D
1C63 66EC 00C3 00C0 0040 05367000 D

1C64 4809 E456 00C0 00C0 05370000 D
1C65 00FC 0000 00C0 00C0 05371000 D
1C66 4809 C052 00C0 00C0 05372000 D
1C67 6819 C0C0 00C0 00C0 05373000 D
1C68 238C 00C3 00C0 00C0 05374000 D
1C69 00C0 00C0 00C0 00C0 05375000 D
1C6A 00C0 00C0 00C0 00C0 05376000 D
1C6B 48C9 EC52 10C0 00C0 05377000 D
1C6C 6330 00C2 00C0 00C0 05378000 D
1C6D 4809 00C0 00C0 00C0 05379000 D
1C6E 0000 00C0 00C0 00C0 05380000 D
1C6F 4809 CC41 00C0 00C0 05381000 D
1C70 4809 E0C1 10C0 00C0 05382000 D
1C71 4809 E003 9070 10C0 05383000 D
1C72 4809 EC52 10C0 00C0 05384000 D
1C73 4809 E0C0 8830 00C0 05385000 D
1C74 30FC 00C0 00C0 00C0 05386000 D
1C75 4809 2C55 00C0 00C0 05387000 D
1C76 51C0 00C3 00C0 00C0 05388000 D

```

OP272:

```

REGSTACK - 1 = CPCR
BMR L = BMR
CONTENTS - 1 = SAR
EINPUB - 1 = CPCR
B L = A2 = SAR
COMP 16 = SAR
BMR + 1 = B
REGSTACK - 1 = CPCR
EINPUB - 1 = CPCR
A2 OR B = A2
A3 AND LIT = 0
REGSTACK - 1 = CPCR
EINPUB - 1 = CPCR
B L = BR2
COMP 8 = SAR
EINPUB - 1 = CPCR
EINPUB - 1 = CPCR
DIV - 1 = CPCR
IF LCL THEN SET LCL
SETOVBIT - 1 = CPCR
IF LCL THEN SKIP
CLEAROV - 1 = CPCR
A2 = MIR
A3 = 0
ASRCCA - 1 = CPCR
BMR R = MAR2
R = SAR
EINPUB - 1 = CPCR
A3 = MIR
BMR + 1 = B
REGSTACK - 1 = CPCR
EINPUB - 1 = CPCR
OPCODE - 1 = MPCR

A3 AND LIT = B
15 = LIT
IF TRUE THEN SKIP
CONTENTS - 1 = CPCR
B L = B
EINPUB - 1 = A3
EINPUB - 1 = CPCR
A2 = SAR
A3 = A2
A2 + B L = B
A3 L = A3
A3 R = A3
A3 OR B = A3
A3 R = B
4 = SAR, 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR

```



```

1C77 4809 0C31 0030 00F0
1C78 0000 0000 0000 0000
1C79 2F30 0000 0000 0000
1C7A 4809 0C31 2000 00F0
1C7B 0000 0000 0000 0000
1C7C 4809 0C31 0000 00F0
1C7D 3100 0000 0000 0000
1C7E 2F30 0000 0000 0000
1C7F 4809 0C31 2000 00F0
1C80 49C9 0000 0000 0000
1C81 0000 0000 0000 0000
1C82 4809 0C31 0000 00F0
1C83 2800 0000 0000 0000
1C84 2800 0000 0000 0000
1C85 50AC 0000 0000 0000
1C86 2819 0000 0000 0000
1C87 5050 0000 0000 0000
1C88 4809 0C31 0000 00F0
1C89 2C00 0000 0000 0000
1C8A 4809 0C31 0000 00F0
1C8B 48C9 0000 0000 0000
1C8C 3000 0000 0000 0000
1C8D 2F30 0000 0000 0000
1C8E 5050 0000 0000 0000
1C8F 4809 0C31 0000 00F0
1C90 2F30 0000 0000 0000
1C91 2F30 0000 0000 0000
1C92 56E9 0000 0000 0000

```

0P2731:

```

1C93 570C 00C3 0000 0000
1C94 4809 0C31 0010 00F0
1C95 0000 00C3 0000 0000
1C96 60E9 0000 0000 0000
1C97 4809 0C40 0030 00F0
1C98 4809 0C00 0000 0000
1C99 30C0 0000 0000 0000
1C9A 4809 2C50 0000 0000
1C9B 51CC 0000 0000 0000
1C9C 4809 0C31 0000 00F0
1C9D 0000 0000 0000 0000
1C9E 2F30 0000 0000 0000
1C9F 4809 0C31 2000 00F0
1CA0 0000 0000 0000 0000
1CA1 5050 0000 0000 0000
1CA2 2F30 0000 0000 0000
1CA3 4809 0C50 2000 00F0
1CA4 49C9 0000 0000 0000
1CA5 4809 0C31 0000 00F0
1CA6 4809 0C31 0000 00F0
1CA7 20C0 0000 0000 0000
1CA8 2800 0000 0000 0000
1CA9 50AC 0000 0000 0000
1CAB 2819 0000 0000 0000
1CAC 5050 0000 0000 0000
1CAD 4809 0C31 0000 00F0
1CAE 2000 0000 0000 0000

```

```

BMAR L = BR1
COMP 0 = SAR
EINPUT - 1 = CPCR
B L = A2
COMP 16 = SAR
BMAR + 1 = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
A2 OR B = A2
A3 R = B SET LC1
16 = SAR
B L = B
DIV - 1 = CPCR
IF LC1 THEN SET LC1
SETOVBIT - 1 = CPCR
IF LC1 THEN SKIP
CLEAROV - 1 = CPCR
A3 = B
SEITCCA - 1 = CPCR
A2 = MIR, ASR
BMAR R = MAR2
6 = SAR
EINPUT - 1 = CPCR
BMAR + 1 = B
REGSTACK - 1 = CPCR
A3 = MIR
EINPUT - 1 = CPCR
OPCODE - 1 = MPCR

RXHFIELD - 1 = CPCR
B L = BR2
COMP 0 = SAR
EMULIN - 1 = CPCR
B = MIR
A3 R = B
4 = SAR, 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
BMAR L = BR1
COMP 0 = SAR
EINPUT - 1 = CPCR
B L = A2
COMP 16 = SAR
BMAR + 1 = B
REGSTACK - 1 = CPCR
A2 OR B = A2
EMULI SET LC1
B L = B
COMP 16 = SAR
DIV - 1 = CPCR
IF LC1 THEN SET LC1
SETOVBIT - 1 = CPCR
IF LC1 THEN SKIP
CLEAROV - 1 = CPCR
A3 = B
SEITCCA - 1 = CPCR

```

% TEMP STORAGE

```

% (R(A+1)) INTO E
% (R(A+1)) INTO MAR2
% (R(A+1)) INTO B
% A2 = (R(A+1))/(R(A+1))
% Y INTO B
% LEFT JUSTIFY DIVISOR
% (R(A+1))/(R(A+1))
% SET THE OV BIT
% CLEAR THE OV BIT
% QUOTIENT FOR SET CC
% SET THE CONDITION BITS
% REMAINDER INTO MIR
% R(A)
% P(A+1)
% R(A+1) INTO MAR2
% QUOTIENT INTO MIR
% TYPE RX DIVIDE, (R(A+1))/(Y) =
% Y INTO B
% R(A+1), REMAINDER INTO R(A), SET OV,
% (Y) INTO B
% ISOLATE "A"
% (R(A) INTO MAR2
% TEMP STORAGE
% (R(A) INTO E
% (R(A+1)) INTO MAR2
% (R(A+1)) INTO B
% A2 = (R(A+1))/(R(A+1))
% LEFT JUSTIFY THE DIVISOR
% (R(A+1))/(Y)
% SET THE OV BIT
% CLEAR THE OV BIT
% QUOTIENT INTO B
% SET THE CONDITION BITS

```


[illegible]


```

10C0 4809 0C41 0000 00F0 00518000 0
10C1 0000 0000 0000 0000 00519000 0
10C2 4809 EC5C 1000 00F0 00520000 0
10C3 633C 0000 0000 0000 00521000 0
10C4 4809 E000 AC00 0000 00522000 0
10C5 4809 E000 AC00 0000 00523000 0
10C6 4809 C640 0000 0000 00524000 0
10C7 4809 E0C3 0920 0000 00525000 0
10C8 2200 0000 0000 0000 00526000 0
10C9 4809 C650 0000 0000 00527000 0
10CA 2F5C 0000 0000 0000 00528000 0
10CB 2000 0000 0000 0000 00529000 0
10CC 64EC C0C0 0000 0000 00530000 0
10CD 570C 0000 0000 0000 00531000 0
10CE 4809 0C41 0C10 00F0 00532000 0
10CF 0000 0000 0000 0000 00533000 0
10D0 60E0 0000 0000 0000 00534000 0
10D1 4809 EC40 0030 0000 00535000 0
10D2 4809 EC00 0000 0000 00536000 0
10D3 2200 0000 0000 0000 00537000 0
10D4 4809 0C40 2000 0000 00538000 0
10D5 4809 C650 0000 0000 00539000 0
10D6 2F5C 0000 0000 0000 00540000 0
10D7 2000 0000 0000 0000 00541000 0
10D8 56E0 0000 0000 0000 00542000 0
10D9 5F9C 0000 0000 0000 00543000 0
10DA 4809 C640 0000 0000 00544000 0
10DB 193C 0000 0000 0000 00545000 0
10DC 4809 00C0 0000 0000 00546000 0
10DD 4824 00C3 0000 0000 00547000 0
10DE 194C 00C3 0000 0000 00548000 0
10DF 195C 00C3 0000 0000 00549000 0
10E0 196C 00C3 0000 0000 00550000 0
10E1 197C 00C3 0000 0000 00551000 0
10E2 220C 0000 0000 0000 00552000 0
10E3 4809 0C40 0030 0000 00553000 0
10E4 2200 0000 0000 0000 00554000 0
10E5 4809 E0C3 0920 0000 00555000 0
10E6 2F5C 0000 0000 0000 00556000 0
10E7 2000 0000 0000 0000 00557000 0
10E8 56E0 0000 0000 0000 00558000 0
10E9 5F9C 0000 0000 0000 00559000 0
10EA 4809 0C41 0C10 00F0 00560000 0
10EB 0000 0000 0000 0000 00561000 0
10EC 238C 00C3 0000 0000 00562000 0
10ED 4809 EC40 2000 0000 00563000 0
10EE 4809 E0C3 0920 0000 00564000 0
10EF 4809 E0C3 0920 0000 00565000 0
10F0 2200 0000 0000 0000 00566000 0
10F1 4809 0C40 0030 0000 00567000 0
10F2 2200 0000 0000 0000 00568000 0
10F3 4809 E0C3 0920 0000 00569000 0
10F4 2F5C 0000 0000 0000 00570000 0
10F5 2000 0000 0000 0000 00571000 0
10F6 56E0 0000 0000 0000 00572000 0
10F7 5F9C 0000 0000 0000 00573000 0
10F8 4809 0C41 0C10 00F0 00574000 0
10F9 0000 0000 0000 0000 00575000 0
10FA 238C 00C3 0000 0000 00576000 0
10FB 4809 EC40 2000 0000 00577000 0
10FC 4809 E0C3 0920 0000 00578000 0
10FD 2200 0000 0000 0000 00579000 0
10FE 4809 0C40 0030 0000 00580000 0
10FF 2200 0000 0000 0000 00581000 0
1100 4809 0C40 0030 0000 00582000 0
1101 238C 00C3 0000 0000 00583000 0
1102 4809 EC40 2000 0000 00584000 0
1103 4809 E0C3 0920 0000 00585000 0
1104 2200 0000 0000 0000 00586000 0
1105 4809 0C40 0030 0000 00587000 0
1106 2F5C 0000 0000 0000 00588000 0
1107 2000 0000 0000 0000 00589000 0
1108 56E0 0000 0000 0000 00590000 0

```

B L = B
 COMP 16 = SAR
 A3 OR B = A3
 IFETCH - 1 = CPCR
 A3 R = A2
 A5 = SAR
 A5 = MIR
 A3 = B
 CONTENTSRA - 1 = CPCR
 B = A2, BHI
 A2 AND B = MIR, B
 EOUTPUT - 1 = CPCR
 SEICCA - 1 = CPCR
 OPCODE - 1 = MPCR

0P3C3:
 PXFIELD - 1 = CPCR
 B L = BR2
 COMP B = SAR
 EMULIN - 1 = CPCR
 B = MIR
 A3 = B
 CONTENTSRA - 1 = CPCR
 B = A2, BHI
 A2 AND B = MIR, B
 EOUTPUT - 1 = CPCR
 SEICCA - 1 = CPCR
 OPCODE - 1 = MPCR

0P31F:
 XFCODE - 1 = CPCR
 A2 + AMPCR = AMPCR
 0P31F - 1 = AMPCR
 STEP
 EXEC

0P31F:
 0P310 - 1 = MPCR
 0P311 - 1 = MPCR
 0P312 - 1 = MPCR
 0P313 - 1 = MPCR

0P310:
 CONTENTSRA - 1 = CPCR
 B = MIR
 CONTENTSRA - 1 = CPCR
 B = A2, BHI
 A2 OR B = MIR, B
 A3 R = MIR
 EOUTPUT - 1 = CPCR
 SEICCA - 1 = CPCR
 OPCODE - 1 = MPCR

0P311:
 RI TYPE 2 OR (INDIRECT)
 (R(A)) OR (Y*) = R(A), SET CC

1109	233C 0000 0000 0000	CONTENTSIRH - 1 = CPCR	% Y = INTO B	05578000 0
110A	4809 0C41 0010 0000	B L = BR2		05575000 0
110B	000C 0000 0000 0000	COMP 8 = SAR		05580000 0
110C	50E0 0000 0000 0000	EMULIN - 1 = CPCR	% (Y*) INTO B	05581000 0
110D	4809 0C43 0000 0000	B = MIR		05582000 0
110E	4809 0C00 0800 0000	A3 = B		05583000 0
110F	2280 0000 0000 0000	CONTENTSRA - 1 = CPCR	% (R(A*)) INTO B	05584000 0
110G	4809 0C40 2000 0000	B = A2, BHI		05585000 0
1110	4809 0C50 0800 0000	A2 OR B = MIR, B		05586000 0
1111	4809 0C5C 0800 0000	EQUIPUT - 1 = CPCR	% SET THE CONDITION BITS	05587000 0
1112	2F5C 0000 0000 0000	SETCCA - 1 = CPCR		05588000 0
1113	2000 0000 0000 0000	OPCODE - 1 = MPCR		05589000 0
1114	56E0 0000 0000 0000			05590000 0
1115	4809 2C55 0800 0000	LIT AND B = 0		05591000 0
1116	000C 0000 0000 0000	I5 = LIT		05592000 0
1117	4809 0C52 0000 0000	0 EOL R	% (R(A)) OR (CONSTANT)	05593000 0
1118	6810 0000 0000 0000	IF TRUE THEN SKIP	% ISOLATE *M*	05594000 0
1119	2380 0000 0000 0000	CONTENTSIRH - 1 = CPCR	% CHECK FOR M = 0	05595000 0
111A	4809 0C41 0800 0000	B L = B	% (R(P*)) INTO B	05596000 0
111B	0000 0000 0000 0000	COMP 16 = SAR		05597000 0
111C	4809 0C5C 1000 0000	A3 OR B = A3		05598000 0
111D	6330 0000 0000 0000	IFETCH - 1 = CPCR	% A3 = (R(P*)) INSTRUCTION	05599000 0
111E	4809 0C00 0000 0000	A3 R = A2	% *Y* INTO B	05600000 0
111F	0CFC 0000 0000 0000	16 = SARI 15 = LIT		05601000 0
1120	4809 0C40 0000 0000	A2 + B = MIR	% Y INTO MIR	05602000 0
1121	4809 0C00 0000 0000	A3 = B		05603000 0
1122	2280 0000 0000 0000	CONTENTSRA - 1 = CPCR	% (R(A*)) INTO B	05604000 0
1123	4809 0C40 2000 0000	B = A2, BHI		05605000 0
1124	4809 0C5C 0800 0000	A2 OR B = MIR, B		05606000 0
1125	2F5C 0000 0000 0000	EQUIPUT - 1 = CPCR		05607000 0
1126	2000 0000 0000 0000	SETCCA - 1 = CPCR	% SET THE CONDITION BITS	05608000 0
1127	56E0 0000 0000 0000	OPCODE - 1 = MPCR		05609000 0
1128	570C 0000 0000 0000			05610000 0
1129	4809 0C41 0010 0000	RYMFIELD - 1 = LPCR	% (R(A)) OR (Y) = (R(A)), SET CC	05611000 0
112A	000C 0000 0000 0000	B L = BR2	% Y INTO B	05612000 0
112B	60E0 0000 0000 0000	COMP 8 = SAR		05613000 0
112C	4809 0C40 0000 0000	EMULIN - 1 = CPCR	% (Y) INTO B	05614000 0
112D	4809 0C00 0800 0000	B = MIR		05615000 0
112E	2280 0000 0000 0000	A3 = B		05616000 0
112F	4809 0C40 2000 0000	CONTENTSRA - 1 = CPCR	% (R(A*)) INTO B	05617000 0
1130	4809 0C5C 0800 0000	B = A2, BHI		05618000 0
1131	2F50 0000 0000 0000	A2 OR B = MIR, B		05619000 0
1132	2000 0000 0000 0000	EQUIPUT - 1 = CPCR	% SET THE CONDITION BITS	05620000 0
1133	56E0 0000 0000 0000	SETCCA - 1 = CPCR		05621000 0
1134	5F9C 0000 0000 0000	OPCODE - 1 = MPCR		05622000 0
1135	4809 0C40 0010 0000			05623000 0
1136	000C 0000 0000 0000	RYMFIELD - 1 = LPCR	% (R(A)) OR (Y) = (R(A)), SET CC	05624000 0
1137	1809 0000 0000 0000	B L = BR2	% Y INTO B	05625000 0
1138	4824 0000 0000 0000	COMP 8 = SAR	% (Y) INTO B	05626000 0
1139	1990 0000 0000 0000	EMULIN - 1 = CPCR	% (Y) INTO B	05627000 0
1140	4809 0C40 0000 0000	B = MIR		05628000 0
1141	2280 0000 0000 0000	A3 = B		05629000 0
1142	4809 0C40 2000 0000	CONTENTSRA - 1 = CPCR	% (R(A*)) INTO B	05630000 0
1143	4809 0C5C 0800 0000	B = A2, BHI		05631000 0
1144	2F50 0000 0000 0000	A2 OR B = MIR, B		05632000 0
1145	2000 0000 0000 0000	EQUIPUT - 1 = CPCR	% SET THE CONDITION BITS	05633000 0
1146	56E0 0000 0000 0000	SETCCA - 1 = CPCR		05634000 0
1147	5F9C 0000 0000 0000	OPCODE - 1 = MPCR		05635000 0
1148	4809 0C40 0010 0000			05636000 0
1149	1990 0000 0000 0000	RYMFIELD - 1 = LPCR	% (R(A)) OR (Y) = (R(A)), SET CC	05637000 0

113A 19A0 00C0 C0C0 C040
113B 19B0 00D0 D0D0 C040
113C 19C0 00E0 E0E0 C040

OP320:

113D 2280 C0C0 00D0 0060
113E 4809 0C40 00D0 0060
113F 238C 00D0 00C0 0060
1140 4809 0C40 20D0 0060
1141 4809 CC4C 004C 0060
1142 4809 C0D0 801C 0060
1143 00C0 00C0 00D0 0020
1144 2F5C 00D0 C0D0 0060
1145 20D0 C0D0 00D0 0060
1146 56E0 00D0 00D0 0040

OP321:

1147 2380 00C0 00D0 C040
1148 4809 0C40 001C C040
1149 00C0 C0D0 00D0 C040
114A 50E0 D0C0 00D0 004C
114B 4809 CC4C 00C0 0060
114C 4809 E0C0 00D0 0060
114D 228C 00C0 00D0 0060
114E 4809 0C40 20D0 0060
114F 4809 CC4C 004C 0060
1150 2F5C C0D0 00D0 0060
1151 20D0 00D0 00D0 C040
1152 56E0 00D0 00D0 C040

OP322:

1153 4809 2C55 00D0 0060
1154 00FC 00C0 00D0 C040
1155 4809 0C52 00D0 0060
1156 5819 00C0 00D0 0060
1157 238C 00C0 00D0 C040
1158 48C9 CC4C 00D0 C040
1159 00C0 C0C0 00D0 0020
115A 00C0 C0C0 00D0 C040
115B 5330 00C0 00D0 0060
115C 4809 E0C0 00D0 C040
115D 00D0 00D0 00D0 0060
115E 48C9 C0C0 00D0 0060
115F 4809 E0C0 00D0 0060
1160 2280 C0C0 00D0 0060
1161 4809 0C40 20D0 0060
1162 4809 CC4C 004C 0060
1163 2F5C 00C0 00C0 0060
1164 20D0 00D0 00D0 C040
1165 66E0 00D0 C0C0 C040

OP323:

OP321 - 1 = MPCR
OP322 - 1 = MPCR
OP323 - 1 = MPCR

OP320:

CONTENTSRA - 1 = CPCR
B = M1R
CONTENTSRRM - 1 = CPCR
B = A2, BHI
A2 XOR B = M1R, F
A3 R = MAR2
16 = SAR
EQUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
OPCODE - 1 = MPCR

OP321:

CONTENTSRRM - 1 = CPCR
B = M1R
COMB B = SAR
EQUIPUT - 1 = CPCR
B = M1R
A3 = B
CONTENTSRA - 1 = CPCR
B = A2, BHI
A2 XOR B = M1R, F
EQUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
OPCODE - 1 = MPCR

OP322:

LIT AND B = B
15 = LIT
0 EOL B
IF TRUE THEN SKIP
CONTENTSRRM - 1 = CPCR
B L = B
COMB 16 = SAR
A3 OR B = A3
EQUIPUT - 1 = CPCR
12 R SAR, 15 = LIT
A2 + B = M1R
A3 = B
CONTENTSRA - 1 = CPCR
B = A2, BHI
A2 XOR B = M1R, F
EQUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
OPCODE - 1 = MPCR

OP323:

05639C00 0
05640C00 0
05641C00 0
05642C00 0
05643C00 0
05644C00 0
05645C00 0
05646C00 0
05647C00 0
05648C00 0
05649C00 0
05650C00 0
05651C00 0
05652C00 0
05653C00 0
05654C00 0
05655C00 0
05656C00 0
05657C00 0
05658C00 0
05659C00 0
05660C00 0
05661C00 0
05662C00 0
05663C00 0
05664C00 0
05665C00 0
05666C00 0
05667C00 0
05668C00 0
05669C00 0
05670C00 0
05671C00 0
05672C00 0
05673C00 0
05674C00 0
05675C00 0
05676C00 0
05677C00 0
05678C00 0
05679C00 0
05680C00 0
05681C00 0
05682C00 0
05683C00 0
05684C00 0
05685C00 0
05686C00 0
05687C00 0
05688C00 0
05689C00 0
05690C00 0
05691C00 0
05692C00 0
05693C00 0
05694C00 0
05695C00 0
05696C00 0
05697C00 0


```

1292 2160 0000 0000 C060
1293 4809 0001 2000 C0FF
1294 2000 0000 0000 0000
1295 4809 C5C0 8800 C0F0
1296 0000 0000 0000 0000
1297 4809 0000 0000 C0FF
1298 6100 0000 0000 C060
1299 6600 0000 C000 0040
129A 4809 A001 C000 00F0
129B 4809 A00F C000 003C
129C 4809 A00F C000 003C
129D 4809 0001 8800 00F0
129E 4809 0000 0000 C030
129F 4809 2000 8C00 00F0
12A0 2030 C000 0000 0040
12A1 4809 E0C0 C610 00F0
12A2 6100 0000 0000 C060
12A3 6600 0000 0000 C040

12A4 3000 0000 0000 C040

12A5 4E00 0000 0000 0040

12A6 5F00 0000 0000 006C
12A7 4809 C000 0000 C0F0
12A8 6806 0000 0000 C0F0
12A9 1A0C 0000 0000 0040
12AA 4809 0000 8800 C0FF
12AB 900C 0000 C000 C080
12AC 4809 2000 2800 00F0
12AD 4809 2000 2800 00F0
12AE 0000 0000 C000 C0E0
12AF 7819 0000 C000 C0F0
12B0 3000 C000 0000 C040
12B1 4809 C640 0000 00F0
12B2 1A0C 0000 0000 C000
12B3 4809 0000 0000 00F0
12B4 4824 0000 0000 00F0

12B5 1800 0000 0000 0040
12B6 1810 0000 0000 C040
12B7 1820 0000 0000 C040
12B8 1830 0000 0000 0040
12B9 1840 0000 0000 C040
12BA 1850 0000 0000 C04C
12BB 4E00 0000 C000 C040
12BC 4E00 0000 C000 0040
12BD 1860 0000 0000 0040
12BE 1870 0000 0000 0040
12BF 1880 0000 0000 0040
12C0 1890 0000 0000 0040

12C1 2260 0000 0000 0060

```

```

% SET THE CONDITION BITS
% SET BIT 14 OF (Y)
% RESTORE Y INTO BR2
% PUT CC DIT 9 INTO LS BIT
% SET BIT 9 TO 0, AND RESTORE A1
% SET (Y) DIT 14,15
% RESTORE Y INTO BR2
% NOT IMPLEMENTED
% THIS ROUTINE ANALYZES THE 4th OP CODE
% IF FIELD RETURNED IN A2
% SPECIAL CASE 404
% ISOLATE THE 14th FIELD
% B AND A2 = 14th FIELD
% TEST FOR NOT ASSIGNED INST.
%
% CC INDICATES = 00 01 JUMP EQUAL
% CC RETURNED IN B

```

```

OPCODE36:
    FAULT - 1 = MPCR
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE37:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE40:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE41:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE42:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE43:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE44:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE45:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```

```

OPCODE46:
    N0TIMP - 1 = MPCR
    XCODE - 1 = CPCR
    IF TRUE THEN STEP ELSE SKIP
    OP40X01 - 1 = MPCR
    B R = B
    4 = SARI 15 = LIT
    LIT AND B = B/A2
    12 = LIT
    IF TRUE THEN SKIP
    FAULT - 1 = MPCR
    A2 + AMPCR = AMPCR
    JUMP40 - 1 = AMPCR
    STEP
    EXEC
    OP40X00 - 1 = MPCR
    OP40X01 - 1 = MPCR
    OP40X02 - 1 = MPCR
    OP40X03 - 1 = MPCR
    OP40X04 - 1 = MPCR
    OP40X05 - 1 = MPCR
    N0TIMP - 1 = MPCR
    OP40X10 - 1 = MPCR
    OP40X11 - 1 = MPCR
    OP40X12 - 1 = MPCR
    OP40X13 - 1 = MPCR
    CHECKCC - 1 = CPCR
    OP40X00:

```



```

1702 4809 0C52 0000 00F0 0 00L B
1703 63C9 0000 0000 00F0 IF FALSE THEN SET LCI
1704 18A0 0000 003C 00A0 OP40X - 1 = MPGR

OP40X01: CHECKCC - 1 = CPCR
0 0118C00 0
0 0119C00 0
0 0120C00 0
0 0121C00 0
0 0122C00 0
0 0123C00 0
0 0124C00 0
0 0125C00 0
0 0126C00 0
0 0127C00 0
0 0128C00 0
0 0129C00 0
0 0130C00 0
0 0131C00 0
0 0132C00 0
0 0133C00 0
0 0134C00 0
0 0135C00 0
0 0136C00 0
0 0137C00 0
0 0138C00 0
0 0139C00 0
0 0140C00 0
0 0141C00 0
0 0142C00 0
0 0143C00 0
0 0144C00 0
0 0145C00 0
0 0146C00 0
0 0147C00 0
0 0148C00 0
0 0149C00 0
0 0150C00 0
0 0151C00 0
0 0152C00 0
0 0153C00 0
0 0154C00 0
0 0155C00 0
0 0156C00 0
0 0157C00 0
0 0158C00 0
0 0159C00 0
0 0160C00 0
0 0161C00 0
0 0162C00 0
0 0163C00 0
0 0164C00 0
0 0165C00 0
0 0166C00 0
0 0167C00 0
0 0168C00 0
0 0169C00 0
0 0170C00 0
0 0171C00 0
0 0172C00 0
0 0173C00 0
0 0174C00 0
0 0175C00 0
0 0176C00 0
0 0177C00 0

% CC NOT EQUAL OR NOT 0, JUMP NOT EQUAL
% CC >= OR + J JUMP GTR OR EQUAL
% CC < OR - J JUMP LESS

OP40X02: CHECKCC - 1 = CPCR
LIT GE0 B
2 = LIT
IF FALSE THEN SET LCI
OP40X - 1 = MPGR

OP40X03: CHECKCC - 1 = CPCR
LIT EOL E
3 = LIT
IF FALSE THEN SET LCI
OP40X - 1 = MPGR

% IF OVERFLOW SET, JUMP, JUMP OVERFLOW

OP40X04: A1 R = A2
27 = SAR
A2
IF NOT LST THEN SET LCI
OP40X - 1 = MPGR

% IF CARRY, JUMP CARRY

OP40X05: A1 R = A2
28 = SAR
A2
IF NOT LST THEN SET LCI
OP40X - 1 = MPGR

% JUMP

OP40X10: OP40X - 1 = MPGR

% JUMP AFTER STOP
% MACHINE STOPS

OP40X11: WAIT
STEP
OP40X - 1 = MPGR

% IF KEY 1 SET, STOP, JUMP.

OP40X12: A1 R = A2
29 = SAR
A2
IF NOT LST THEN SET LCI ELSE SKIP
OP40X - 1 = MPGR

% MACHINE STOPS
WAIT
STEP
OP40X - 1 = MPGR

% IF KEY 2 SET, STOP, JUMP

OP40X13: A1 R = A2
30 = SAR
A2

```


124C	51C0	07C0	00C0	00C0	IF NOT LST THEN SET LC1 ELSE SKIP	06170000
124D	5819	00C0	00C0	00C0	IF LST THEN SKIP	06170100
124E	1C40	07C0	00C0	00C0	OP40X - 1 = MPCR	06170200
124F	4800	00C0	00C0	00C0	WAIT	06170300
124G	4800	00C0	00C0	00C0	MACHINE STOPS	06170400
124H	4809	00C0	00C0	00C0	STEP	06182100
124I	1C5C	00C0	00C0	00C0	OP40X - 1 = MPCR	06182200
124J	5F9C	00C0	00C0	00C0	%	06182300
124K	4309	C640	C0C0	C0C0	% DECODE THE IF1 FIELD	06182400
124L	1C6C	C0C0	00C0	00C0	A2 + AMPCR = AMPCR	06182500
124M	4809	00C0	C0C0	C0C0	OP40F - 1 = AMPCR	06182600
124N	4024	C0C0	00C0	00C0	STEP	06182700
124O	1C7C	00C0	00C0	00C0	EXEC	06182800
124P	5F9C	00C0	00C0	00C0	%	06182900
124Q	4309	C640	C0C0	C0C0	OP400 - 1 = MPCR	06190000
124R	1C6C	C0C0	00C0	00C0	FAULT - 1 = MPCR	06190100
124S	4809	00C0	C0C0	C0C0	OP402 - 1 = MPCR	06190200
124T	4024	C0C0	00C0	00C0	OP403 - 1 = MPCR	06190300
124U	1C7C	00C0	00C0	00C0	%	06190400
124V	5F9C	00C0	00C0	00C0	OP400 - 1 = MPCR	06190500
124W	4309	C640	C0C0	C0C0	FAULT - 1 = MPCR	06190600
124X	1C6C	C0C0	00C0	00C0	OP402 - 1 = MPCR	06190700
124Y	4809	00C0	C0C0	C0C0	OP403 - 1 = MPCR	06190800
124Z	4024	C0C0	00C0	00C0	%	06190900
124A	1C7C	00C0	00C0	00C0	OP400 - 1 = MPCR	06191000
124B	5F9C	00C0	00C0	00C0	FAULT - 1 = MPCR	06191100
124C	4309	C640	C0C0	C0C0	OP402 - 1 = MPCR	06191200
124D	4024	C0C0	00C0	00C0	OP403 - 1 = MPCR	06191300
124E	1C7C	00C0	00C0	00C0	%	06191400
124F	5F9C	00C0	00C0	00C0	OP400 - 1 = MPCR	06191500
124G	4309	C640	C0C0	C0C0	FAULT - 1 = MPCR	06191600
124H	1C6C	C0C0	00C0	00C0	OP402 - 1 = MPCR	06191700
124I	4809	00C0	C0C0	C0C0	OP403 - 1 = MPCR	06191800
124J	4024	C0C0	00C0	00C0	%	06191900
124K	1C7C	00C0	00C0	00C0	OP400 - 1 = MPCR	06192000
124L	5F9C	00C0	00C0	00C0	FAULT - 1 = MPCR	06192100
124M	4309	C640	C0C0	C0C0	OP402 - 1 = MPCR	06192200
124N	4024	C0C0	00C0	00C0	OP403 - 1 = MPCR	06192300
124O	1C7C	00C0	00C0	00C0	%	06192400
124P	5F9C	00C0	00C0	00C0	OP400 - 1 = MPCR	06192500
124Q	4309	C640	C0C0	C0C0	FAULT - 1 = MPCR	06192600
124R	1C6C	C0C0	00C0	00C0	OP402 - 1 = MPCR	06192700
124S	4809	00C0	C0C0	C0C0	OP403 - 1 = MPCR	06192800
124T	4024	C0C0	00C0	00C0	%	06192900
124U	1C7C	00C0	00C0	00C0	OP400 - 1 = MPCR	06193000
124V	5F9C	00C0	00C0	00C0	FAULT - 1 = MPCR	06193100
124W	4309	C640	C0C0	C0C0	OP402 - 1 = MPCR	06193200
124X	4024	C0C0	00C0	00C0	OP403 - 1 = MPCR	06193300
124Y	1C7C	00C0	00C0	00C0	%	06193400
124Z	5F9C	00C0	00C0	00C0	OP400 - 1 = MPCR	06193500
124A	4309	C640	C0C0	C0C0	FAULT - 1 = MPCR	06193600
124B	1C6C	C0C0	00C0	00C0	OP402 - 1 = MPCR	06193700
124C	4809	00C0	C0C0	C0C0	OP403 - 1 = MPCR	06193800
124D	4024	C0C0	00C0	00C0	%	06193900
124E	1C7C	00C0	00C0	00C0	OP400 - 1	


```

131E 0000 0000 0000 0020      16 = SAR
131F 4809 AC14 407C 60F0      A1 L = A1
1320 4809 AC5C 407C 60F0      A1 OR D = A1
1321 66E0 0070 0070 0040      OPCODE - 1 = MPCR

OP401:
1322 559C 0070 0070 004C      R11 - 1 = MPCR

OPCODE41:
1323 5F90 00C0 0030 0060      YECODE - 1 = CPCR
1324 4809 C640 007C C0FC      A2 + MPCR = AMPCR
1325 1CAC 0003 C030 00C0      OP41F - 1 = AMPCR
1326 4009 00C0 C00C 00F0      STEP
1327 4824 0063 0070 00FC      EXEC

1328 1CB0 00C0 007C 0040      OP41F:
1329 1CC0 0070 C07C 0040      OP411 - 1 = MPCR
132A 00C0 007C 004C      OP412 - 1 = MPCR
132B 1CEC 0060 000C 0040      OP413 - 1 = MPCR

OP410:
132C 2260 00C0 0070 C060      CONTENTSRA - 1 = CPCR
132D 4809 0052 C030 0060      D EOL 0
132E 56E0 00C0 007C 00F0      IF TRUE THEN STEP ELSE SKIP
132F 56E0 007C 0070 0040      OPCODE - 1 = MPCR
1330 4809 0040 207C 00F0      R = A2
1331 4809 0070 207C 00F0      A2 - 1 = M1R
1332 2E58 C030 007C 0060      OUTPUT - 1 = CPCR
1333 2380 00C0 C00C 0060      IF TRUE THEN STEP ELSE SKIP
1334 1809 00C0 C030 00F0      CONTENTSRA - 1 = CPCR
1335 0000 00C0 007C C020      A1 R = A1
1336 1809 AC14 4000 00F0      16 = SAR
1337 1809 AC5C 407C 00F0      A1 OR D = A1
1338 56E0 00C0 0000 0040      OPCODE - 1 = MPCR

OP411:
1339 2260 00C0 007C 0060      CHECKCC - 1 = CPCR
133A 1809 C0C2 007C C0FC      R EOL 0
133B 680B 00C0 007C 00F0      IF TRUE THEN STEP ELSE SKIP
133C 56E0 00C0 0000 0040      OPCODE - 1 = MPCR
133D 5590 0070 007C C04C      R11 - 1 = MPCR

OP412:
133E 2260 00C0 C030 0060      IF TRUE THEN STEP ELSE SKIP
133F 1809 0052 C030 0060      CONTENTSRA - 1 = CPCR
1340 680B 00C0 007C C0FC      IF TRUE THEN STEP ELSE SKIP
1341 56E0 00C0 007C C04C      OPCODE - 1 = MPCR
1342 4809 0040 207C 00FC      B = A2

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1372 4809 0C40 800C 00F0
1373 50FC 0FC0 000C 008C
1374 4809 2C56 0B30 00FC
1375 510C 00C0 0000 006C
1376 4809 A001 2C00 00F0
1377 4809 C000 0000 0020
1378 4809 C0C0 003C 00FC
1379 4809 C0C0 003C 00FC
137A 2F5C 00C0 00C0 0060
137B 2380 00C3 000C 006C
137C 4809 A0C0 00C0 006C
137D 000C 00C0 00C0 0020
137E 4809 A0C1 40C0 00F0
137F 4809 AC5C 40C0 00F0
1380 66EC 00C0 00C0 0040

1381 4809 0C00 80C0 00FC
1382 80F0 0FC0 000C 008C
1383 4809 2C56 0B30 00FC
1384 510C 00C0 0000 006C
1385 4809 A0C1 20C0 00F0
1386 0020 00C0 00C0 0040
1387 4809 C0C0 AC0C 00F0
1388 4809 C140 00C0 006C
1389 2F5C 00C0 00C0 006C
138A 4809 E356 10C0 00FC
138B 00FC 00C0 00C0 006C
138C 50F0 E012 00C0 00F0
138D 50F0 0000 0000 00FC
138E 4809 0C40 10C0 00FC
138F 4809 0C40 10C0 00FC
1390 633C 00C0 000C 0060
1391 4809 E540 80C0 00F0
1392 4809 A0C3 CC00 00F0
1393 0000 00C0 00C0 0020
1394 4809 A0C1 40C0 00F0
1395 4809 AC5C 40C0 00F0
1396 66EC 0000 00C0 0040

1397 4809 0C40 80C0 00FC
1398 80F0 0C00 00C0 0080
1399 4809 2C56 0B30 00FC
139A 510C 00C0 0000 006C
139B 4809 A0C1 20C0 00F0
139C 0020 00C0 00C0 0040
139D 4809 C0C0 AC0C 00F0
139E 4809 C140 00C0 006C
139F 2F5C 00C0 00C0 006C
139A 4809 A0C1 40C0 00F0
139B 570C 00C0 000C 006C
139C 4809 0C41 0C10 00FC
139D 00C0 00C0 000C 0030
139E 60E0 00C0 00C0 0060

1397 4809 0C40 80C0 00FC
1398 80F0 0C00 00C0 0080
1399 4809 2C56 0B30 00FC
139A 510C 00C0 0000 006C
139B 4809 A0C1 20C0 00F0
139C 0020 00C0 00C0 0040
139D 4809 C0C0 AC0C 00F0
139E 4809 C140 00C0 006C
139F 2F5C 00C0 00C0 006C
139A 4809 A0C1 40C0 00F0
139B 570C 00C0 000C 006C
139C 4809 0C41 0C10 00FC
139D 00C0 00C0 000C 0030
139E 60E0 00C0 00C0 0060

06358C00 0
06359F00 0
06360C00 0
06361C00 0
06362C00 0
06363C00 0
06364C00 0
06365C00 0
06366F00 0
06367C00 0
06368C00 0
06369C00 0
06370C00 0
06371C00 0
06372C00 0
06373C00 0
06374C00 0
06375C00 0
06376C00 0
06377000 0
06378C00 0
06379C00 0
06380C00 0
06381000 0
06382C00 0
06383C00 0
06384C00 0
06385C00 0
06386C00 0
06387C00 0
06388000 0
06389000 0
06390C00 0
06391C00 0
06392C00 0
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06403C00 0
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06405C00 0
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06407C00 0
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06410C00 0
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06413C00 0
06414C00 0
06415C00 0
06416C00 0
06417C00 0

06358C00 0
06359F00 0
06360C00 0
06361C00 0
06362C00 0
06363C00 0
06364C00 0
06365C00 0
06366F00 0
06367C00 0
06368C00 0
06369C00 0
06370C00 0
06371C00 0
06372C00 0
06373C00 0
06374C00 0
06375C00 0
06376C00 0
06377000 0
06378C00 0
06379C00 0
06380C00 0
06381000 0
06382C00 0
06383C00 0
06384C00 0
06385C00 0
06386C00 0
06387C00 0
06388000 0
06389000 0
06390C00 0
06391C00 0
06392C00 0
06393C00 0
06394C00 0
06395C00 0
06396C00 0
06397C00 0
06398C00 0
06399C00 0
06400C00 0
06401C00 0
06402C00 0
06403C00 0
06404C00 0
06405C00 0
06406C00 0
06407C00 0
06408C00 0
06409C00 0
06410C00 0
06411C00 0
06412C00 0
06413C00 0
06414C00 0
06415C00 0
06416C00 0
06417C00 0


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1304 5819 00C0 0000 C0C0
1305 2380 00C0 0030 0060
1306 4809 0C40 10C0 00C0
1307 533C 00C0 C09C 0060
1308 4809 C040 10C0 00C0
1309 00C0 00C0 00C0 C030
1310 0852 C0C0 2C30 C0C0
1311 0852 C0C0 2C30 C0C0
1312 4809 C0C0 40C0 00C0
1313 4809 C140 0030 00C0
1314 51E0 00C0 C020 00C0
1315 4809 E0C0 90C0 00C0
1316 0000 00C0 C0C0 C010
1317 4809 E0C0 0870 C0C0
1318 4809 A0C0 C0C0 00C0
1319 00C0 00C0 00C0 0020
1320 4809 A0C0 40C0 00C0
1321 4809 AC5C 4C70 00C0
1322 56E0 00C0 00C0 C040

IF TRUE THEN SKIP
CONTENTSRM - 1 = CPCR % (R(P)) INTO B
D = A3
IFEICH - 1 = CPCR % Y INTO B
A3 + B L = BR2 + A3
COMP 8 = SAR
A1 L = A2
COMP 16 = SARJ 2 = LIT
A2 + LIT = MIR
EMULOUT - 1 = CPCR
A3 R = A3
A = SAR
A3 + 1 = B
A1 R = A1
16 = SAR
A1 L = A1
A1 OR U = A1
OPCODE - 1 = HPCR

RXMFIELD - 1 = CPCR
B L = BR2 + A3
COMP 8 = SAR
A1 L = A2
COMP 16 = SARJ 2 = LIT
A2 R = A2
A2 + LIT = MIR
EMULOUT - 1 = CPCR
A3 R = A3
B = SAR
A1 R = B
16 = SAR
A1 L = A1
A1 OR B = A1
OPCODE - 1 = HPCR

OPCODE44:
XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP44F - 1 = AMPCR
STEP
EXEC

OP44F:
OP440 - 1 = HPCR
OP441 - 1 = HPCR
OP442 - 1 = HPCR
OP443 - 1 = HPCR

OP440:
CONTENTSRM - 1 = CFCHR
B EOL 0

13E7 570C 00C0 0070 C06C
13E8 48C9 0C40 10C0 00C0
13E9 00C0 00C0 0030 C030
13EA 4809 A0C0 20C0 00C0
13EB 00C0 00C0 0C70 00A0
13EC 4809 C0C0 A0C0 00C0
13ED 48P2 C140 C030 00C0
13EE 41EC C0C0 90C0 0060
13EF 00C0 00C0 00C0 C0F0
13F0 00C0 C0C0 0030 C0F0
13F1 4809 E0C0 0870 00C0
13F2 48C9 A0C0 C030 00C0
13F3 00C0 00C0 00C0 0020
13F4 4809 A0C0 40C0 00C0
13F5 4809 AC5C 40C0 00C0
13F6 56EC 00C0 00C0 C04C

13F7 5F9C C0C0 0030 00C0
13F8 48C9 C640 0C40 00C0
13F9 1D7C 00C0 00C0 00C0
13FA 4809 00C0 0030 C0C0
13FB 4824 00C0 0000 00C0

13FC 1D8C 00C0 0C70 0040
13FD 1D30 00C0 0000 C040
13FE 1D4C 00C0 0C10 0040
13FF 1D80 00C0 C030 0040

1400 228C C0C0 0000 C060
1401 4809 C05C C030 C0C0

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1402 6819 0C30 0C30 00F0
1403 66E0 0C30 00C0 0040
1404 2380 0C30 00C0 006C
1405 4869 A0C0 0C30 00FC
1406 00C0 00C0 0C30 002C
1407 4869 A0C1 4C7C 00F0
1408 4869 AC5C 403C 00FC
1409 56E0 0C30 00C0 004C

IF TRUE THEN SKIP
OPCODE - 1 = MPCR
CONTENISRA - 1 = CPCR
% RETURNS (R(H)) IN B
% CLEAR OLD PAR
AL R = A1
COMP 16 = SAR
AL L = A1
AL R = A1
OPCODE - 1 = MPCR

0P441:
140A 2250 0000 0070 006C
140B 4800 CC52 0C70 00F0
140C 6819 0C30 0C30 00F0
140D 66E0 0C30 0C30 0040
140E 5590 0C30 00C0 0C40

CHECKCC - 1 = CPCR
B EOL 0
IF TRUE THEN SKIP
OPCODE - 1 = MPCR
R11 - 1 = MPCR

% RI TYPE 1 LOCAL JUMP EQUAL
% IF (CC) = 0R 0, (P) + D INTO P
% RETURNS CC BITS IN B
% (P) + D = P
%
% RK TYPE JUMP ZERO
% IF (R(A)) 0, Y INTO P
%
% ADVANCE THE PAR BY 1 AND CALL OPCODE
% "M" FIELD IN A3
%
% SKIP
CONTENISRA - 1 = CPCR
% RETURN (R(H)) IN B
% Y INTO B
% PAR VALUE IN LS WORD OF E
% CLEAR OLD PAR
AL L = A1
AL R = A1
OPCODE - 1 = MPCR

0P442:
1410 2280 0C30 0C30 0060
1411 4809 0C52 007C 00F0
1412 1030 0000 00C0 0C40
1413 4839 E156 1C30 00F0
1414 00F0 0000 0C30 00FC
1415 4819 6C12 0030 00FC
1416 2380 0C30 00C0 00FC
1417 2380 0C30 100C 00F0
1418 4839 0C40 100C 00F0
1419 533C 0000 007C 0060
141A 4809 0C40 0B30 00FC
141B 4809 A0C0 0C30 00FC
141C 00C0 0C30 0C30 002C
141D 4809 A001 4C3C 00F0
141E 4869 AC5C 4C3C 00F0
141F 56E0 00C0 0030 004C

IF TRUE THEN SKIP
PUMP - 1 = MPCR
A3 = 9
R11FIELD - 1 = CPCR
R L = BR2
COMP 8 = SAR
COMP 8 = SAR
AL R = A1
COMP 16 = SAR
AL L = A1
AL R = A1
OPCODE - 1 = MPCR

0P443:
1420 2250 0000 0070 006C
1421 4809 0C52 0C30 00F0
1422 6819 0000 00C0 00F0
1423 103C 0000 00C0 0C40
1424 4809 0C30 0B30 00F0
1425 5700 0000 0030 006C
1426 4809 0C41 0C1C 00FC
1427 00C0 00C0 0C30 0C30
1428 50E0 0C30 0C30 0060
1429 4809 0C30 0000 00FC
142A 4809 0C30 0000 002C
142B 4809 AC5C 4C3C 00F0
142C 4809 AC5C 4C3C 00F0
142D 56E0 0000 0070 004C

% JUMP NOT ZERO
% RETURN "M" FIELD IN LSD OF A2

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142F	4809 C640 0000 0000	A2 + AMPCR = AMPCR	06539800 0
1430	10C0 C0C0 0000 0000	OP45F - 1 = AMPCR	06559700 0
1431	4809 0000 0000 C0F0	STEP	0660C000 0
1432	4824 00C0 0000 C0F0	EXLC	06601C00 0
1433	1000 0000 C000 0000	OP45F:	06602C00 0
1434	10E0 00C0 0000 0000	OP451 - 1 = MPCR	06613C00 0
1435	10F0 00C0 0000 C000	OP451 - 1 = MPCR	06604C00 0
1436	1E00 C000 00C0 C000	OP452 - 1 = MPCR	06605C00 0
1437	220C 00C0 00C0 0000	OP453 - 1 = MPCR	06606C00 0
1438	4809 C0C2 0000 0000	OP450:	06607C00 0
1439	500E 00C0 0000 0000	CONTENISRA - 1 = CPCR	06608C00 0
1440	55E0 00C0 0000 0000	B EOL 0	06609C00 0
1441	55E0 00C0 0000 0000	IF TRUE THEN STEP ELSE SKIP	06610C00 0
1442	55E0 00C0 0000 0000	OPCODE - 1 = MPCR	06611C00 0
1443	1809 4000 C000 0000	CONTENISRA - 1 = CPCR	06612C00 0
1444	0000 0000 00C0 0020	COMP 16 A1 SAR	06613C00 0
1445	3809 4010 0000 0000	A1 L = A1 SAR	06614C00 0
1446	3809 4010 0000 0000	A1 L = A1 SAR	06615C00 0
1447	3809 4010 0000 0000	A1 L = A1 SAR	06616C00 0
1448	56E0 C000 0000 0000	OPCODE - 1 = MPCR	06617C00 0
1449	226C 00C0 C000 0000	OP451:	06618C00 0
1450	4809 C0C2 0000 0000	OP451:	06619C00 0
1451	4809 C0C2 0000 0000	OP451:	06620C00 0
1452	103C C0C0 0000 0000	OP451:	06621C00 0
1453	4809 E155 0000 0000	OP451:	06622C00 0
1454	00C0 C000 0000 0000	OP451:	06623C00 0
1455	4809 EC12 0000 0000	OP451:	06624C00 0
1456	5019 00C0 0000 0000	OP451:	06625C00 0
1457	238C 0000 0000 0000	OP451:	06626C00 0
1458	5330 0000 0000 0000	OP451:	06627C00 0
1459	4809 EC40 0000 0000	OP451:	06628C00 0
1460	4809 4000 0000 0000	OP451:	06629C00 0
1461	0000 C000 0000 0000	OP451:	06630C00 0
1462	4809 4000 0000 0000	OP451:	06631C00 0
1463	4809 4000 0000 0000	OP451:	06632C00 0
1464	4809 4000 0000 0000	OP451:	06633C00 0
1465	4809 4000 0000 0000	OP451:	06634C00 0
1466	4809 4000 0000 0000	OP451:	06635C00 0
1467	4809 4000 0000 0000	OP451:	06636C00 0
1468	4809 4000 0000 0000	OP451:	06637C00 0
1469	4809 4000 0000 0000	OP451:	06638C00 0
1470	4809 4000 0000 0000	OP451:	06639C00 0
1471	4809 4000 0000 0000	OP451:	06640C00 0
1472	4809 4000 0000 0000	OP451:	06641C00 0
1473	4809 4000 0000 0000	OP451:	06642C00 0
1474	4809 4000 0000 0000	OP451:	06643C00 0
1475	4809 4000 0000 0000	OP451:	06644C00 0
1476	4809 4000 0000 0000	OP451:	06645C00 0
1477	4809 4000 0000 0000	OP451:	06646C00 0
1478	4809 4000 0000 0000	OP451:	06647C00 0
1479	4809 4000 0000 0000	OP451:	06648C00 0
1480	4809 4000 0000 0000	OP451:	06649C00 0
1481	4809 4000 0000 0000	OP451:	06650C00 0
1482	4809 4000 0000 0000	OP451:	06651C00 0
1483	4809 4000 0000 0000	OP451:	06652C00 0
1484	4809 4000 0000 0000	OP451:	06653C00 0
1485	4809 4000 0000 0000	OP451:	06654C00 0
1486	4809 4000 0000 0000	OP451:	06655C00 0
1487	4809 4000 0000 0000	OP451:	06656C00 0
1488	4809 4000 0000 0000	OP451:	06657C00 0
1489	4809 4000 0000 0000	OP451:	06658C00 0
1490	4809 4000 0000 0000	OP451:	06659C00 0
1491	4809 4000 0000 0000	OP451:	06660C00 0
1492	4809 4000 0000 0000	OP451:	06661C00 0
1493	4809 40		


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1439 4809 2C56 0670 00F0 06558E00 0
1440 510C 0070 0070 0060 06659100 0
1441 2F30 0F00 0070 0060 06660100 0
1442 4809 0C52 0000 00F0 06661100 0
1443 4809 0052 0000 00F0 06662100 0
1444 5000 0000 0070 00F0 06663000 0
1445 403C 0070 0070 0060 06664000 0
1446 5700 0070 0070 0060 06665000 0
1447 4809 0C41 0010 00F0 06666000 0
1448 6000 0070 0070 0060 06667000 0
1449 601C 0000 0070 0060 06668000 0
1450 4809 A0C0 C000 00F0 06669000 0
1451 4809 A0C1 403C 00F0 06670000 0
1452 601C 0000 0070 0060 06671000 0
1453 4809 AC5C 403C 00F0 06672000 0
1454 66E0 C000 C000 0040 06673000 0
1455 66E0 C000 C000 0040 06674000 0
1456 5F9C 0000 0000 0060 06675000 0
1457 3809 C640 C070 00F0 06676000 0
1458 1E10 0000 0000 00C0 06677000 0
1459 4809 0000 0030 00F0 06678000 0
1460 4809 0000 0030 00F0 06679000 0
1461 4824 C003 0C7C 00F0 06680000 0
1462 4E20 0000 0070 0090 06681000 0
1463 1E3C 0070 0C00 0090 06682000 0
1464 1E40 0000 0030 0090 06683000 0
1465 1E50 0000 0000 0090 06684000 0
1466 4809 0000 0030 00F0 06685000 0
1467 4809 AC5C 403C 00F0 06686000 0
1468 66E0 C000 C000 0040 06687000 0
1469 66E0 C000 C000 0040 06688000 0
1470 226C 0000 0000 0060 06689000 0
1471 4809 2C52 0C7C 00F0 06690000 0
1472 3809 C640 C070 00F0 06691000 0
1473 4809 0000 0030 00F0 06692000 0
1474 66E0 C000 C000 0040 06693000 0
1475 2380 0000 0000 0060 06694000 0
1476 4809 A0C0 C000 00F0 06695000 0
1477 4809 A0C1 403C 00F0 06696000 0
1478 3000 00C0 0070 0020 06697000 0
1479 4809 AC5C 403C 00F0 06698000 0
1480 66E0 C000 C000 0040 06699000 0
1481 66E0 C000 C000 0040 06700000 0
1482 559C 0000 0000 0060 06701000 0
1483 226C 0000 0000 0060 06702000 0
1484 4809 2C52 0C7C 00F0 06703000 0
1485 3809 C640 C070 00F0 06704000 0
1486 4809 0000 0030 00F0 06705000 0
1487 6800 0000 0000 00C0 06706000 0
1488 66E0 C000 C000 0040 06707000 0
1489 559C 0000 0000 0060 06708000 0
1490 226C 0000 0000 0060 06709000 0
1491 4809 2C52 0C7C 00F0 06710000 0
1492 3809 C640 C070 00F0 06711000 0
1493 4809 0000 0030 00F0 06712000 0
1494 6800 0000 0000 00C0 06713000 0
1495 66E0 C000 C000 0040 06714000 0
1496 559C 0000 0000 0060 06715000 0
1497 226C 0000 0000 0060 06716000 0
1498 4809 2C52 0C7C 00F0 06717000 0

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1484	4809	CC41	0C70	C0F0	B L = B	% SHIFT (RCA) INTO UHW OF B	06778C00 D
1485	0000	00C3	0C70	F02C	COMP 16 = SAR	% PUT B IN THE ADDR, TEST (RCA) < 0	06779C00 D
1486	4809	0C40	0000	00F0	IF RST THEN SKIP		06706C00 D
1487	4819	CC03	007C	C0FC	OPCODE - 1 = MPCR		067F8C00 D
1488	56EC	0C03	0C7C	C0FC	CONTENTSRM - 1 = CPCR	% (RCH) INTO D	067F2C00 D
1489	2380	0000	0000	006C	CONTENTSRM - 1 = CPCR	% CLEAR LOWER 16 BITS OF A1	06783C00 D
1490	4809	AC03	CC50	00FC	COMP 16 = SAR		06794C00 D
1491	0000	00C0	0C7C	F020	A1 L = A1		06785C00 D
1492	4809	AC01	4C20	00F0	A1 OR B = A1	% MODIFY PAR 10 JUMP	06786C00 D
1493	4809	AC5E	4070	C0FC	OPCODE - 1 = MPCR		06787C00 C
1494	56EC	0000	0030	C0FC			06788C00 D
1495	2809	0000	0C3C	C0F0	IF LC1	% RI TYPE 1 LOCAL JUMP LESS INSTRUCTION	06791C00 C
1496	226C	C0C0	0020	C06C	CHECKCC - 1 = CPCR	% IF (CC) = 11, (P) + 0 = 1	06792C00 D
1497	4809	2E52	000C	C0F0	LIT F0L B	% PUT THE CC BITS INTO B	06793C00 D
1498	003C	C0C3	000C	00E0	3 = LIT	% CHECK CC FOR 11	06794C00 D
1499	66CB	C0C0	C030	00F0	IF FALSE THEN STEP ELSE SKIP		06795C00 D
1500	66EC	00C0	C070	0040	OPCODE - 1 = MPCR		06796C00 D
1501	5590	0000	0020	C04C	R11 - 1 = MPCR	% (P) + 0 = P	06797C00 D
1502	228C	00C3	000C	0060	CONTENTSRM - 1 = CPCR	% RK TYPE JUMP NEGATIVE	06800C00 D
1503	4809	0C40	0000	0020	B L = B	% IF (RCA) < 0, (Y) = P	06801C00 D
1504	0000	00C0	007C	C0FC	COMP 16 = SAR	% (RCA) INTO B	06802C00 D
1505	4809	0C40	007C	C0FC	IF RST THEN SKIP	% SHIFT (RCA) INTO UHW OF B	06803C00 D
1506	4819	CC03	007C	C0FC	CONTENTSRM - 1 = CPCR	% CHECK IF (RCA) < 0	06804C00 D
1507	2380	0000	0000	006C	B L = B	% ADVANCE THE PAR BY 1 AND CALL OPCODE	06805C00 D
1508	4809	0C40	007C	C0FC	IF RST THEN SKIP	% (RCH) INTO E	06806C00 D
1509	4809	0C40	007C	C0FC	IF RST THEN SKIP	% PUT Y INTO B	06807C00 D
1510	4809	0C40	007C	C0FC	IF RST THEN SKIP	% PUT PAR VALUE IN LS WORD OF B	06808C00 D
1511	4809	0C40	007C	C0FC	IF RST THEN SKIP	% CLEAR OLD PAR	06809C00 D
1512	4809	0C40	007C	C0FC	IF RST THEN SKIP	% CONSTRUCT NEW PAR	06810C00 D
1513	4809	0C40	007C	C0FC	IF RST THEN SKIP	% RX TYPE JUMP INSTRUCTION	06811C00 D
1514	4809	0C40	007C	C0FC	IF RST THEN SKIP	% IF (RCA) < 0, (Y) = P	06812C00 D
1515	4809	0C40	007C	C0FC	IF RST THEN SKIP	% SHIFT "A" INTO LS BITS OF B	06813C00 D
1516	4809	0C40	007C	C0FC	IF RST THEN SKIP	% ISOLATE "A" INTO B	06814C00 D
1517	4809	0C40	007C	C0FC	IF RST THEN SKIP	% (RCA) INTO MAR2	06815C00 D
1518	4809	0C40	007C	C0FC	IF RST THEN SKIP	% (RCA) INTO E	06816C00 D
1519	4809	0C40	007C	C0FC	IF RST THEN SKIP	% (RCA) SHIFTED INTO UHW OF B	06817C00 D
1520	4809	0C40	007C	C0FC	IF RST THEN SKIP	% CHECK IF (RCA) < 0	06818C00 C
1521	4809	0C40	007C	C0FC	IF RST THEN SKIP	% ADVANCE THE PAR BY 1 AND CALL OPCODE	06819C00 D
1522	4809	0C40	007C	C0FC	IF RST THEN SKIP	% RESTORE INSTRUCTION IN E	06820C00 D
1523	4809	0C40	007C	C0FC	IF RST THEN SKIP	% ANALYZE "M" FIELD	06821C00 D
1524	4809	0C40	007C	C0FC	IF RST THEN SKIP	% PUT Y INTO PAR2	06822C00 D
1525	4809	0C40	007C	C0FC	IF RST THEN SKIP	% PUT (Y) INTO B	06823C00 D
1526	4809	0C40	007C	C0FC	IF RST THEN SKIP		06824C00 D
1527	4809	0C40	007C	C0FC	IF RST THEN SKIP		06825C00 D
1528	4809	0C40	007C	C0FC	IF RST THEN SKIP		06826C00 D
1529	4809	0C40	007C	C0FC	IF RST THEN SKIP		06827C00 D
1530	4809	0C40	007C	C0FC	IF RST THEN SKIP		06828C00 D
1531	4809	0C40	007C	C0FC	IF RST THEN SKIP		06829C00 D
1532	4809	0C40	007C	C0FC	IF RST THEN SKIP		06830C00 D
1533	4809	0C40	007C	C0FC	IF RST THEN SKIP		06831C00 D
1534	4809	0C40	007C	C0FC	IF RST THEN SKIP		06832C00 D
1535	4809	0C40	007C	C0FC	IF RST THEN SKIP		06833C00 D
1536	4809	0C40	007C	C0FC	IF RST THEN SKIP		06834C00 D
1537	4809	0C40	007C	C0FC	IF RST THEN SKIP		06835C00 D
1538	4809	0C40	007C	C0FC	IF RST THEN SKIP		06836C00 D
1539	4809	0C40	007C	C0FC	IF RST THEN SKIP		06837C00 D
1540	4809	0C40	007C	C0FC	IF RST THEN SKIP		06838C00 D
1541	4809	0C40	007C	C0FC	IF RST THEN SKIP		06839C00 D
1542	4809	0C40	007C	C0FC	IF RST THEN SKIP		06840C00 D
1543	4809	0C40	007C	C0FC	IF RST THEN SKIP		06841C00 D
1544	4809	0C40	007C	C0FC	IF RST THEN SKIP		06842C00 D
1545	4809	0C40	007C	C0FC	IF RST THEN SKIP		06843C00 D
1546	4809	0C40	007C	C0FC	IF RST THEN SKIP		06844C00 D
1547	4809	0C40	007C	C0FC	IF RST THEN SKIP		06845C00 D
1548	4809	0C40	007C	C0FC	IF RST THEN SKIP		06846C00 D
1549	4809	0C40	007C	C0FC	IF RST THEN SKIP		06847C00 D
1550	4809	0C40	007C	C0FC	IF RST THEN SKIP		06848C00 D
1551	4809	0C40	007C	C0FC	IF RST THEN SKIP		06849C00 D
1552	4809	0C40	007C	C0FC	IF RST THEN SKIP		06850C00 D
1553	4809	0C40	007C	C0FC	IF RST THEN SKIP		06851C00 D
1554	4809	0C40	007C	C0FC	IF RST THEN SKIP		06852C00 D
1555	4809	0C40	007C	C0FC	IF RST THEN SKIP		06853C00 D
1556	4809	0C40	007C	C0FC	IF RST THEN SKIP		06854C00 D
1557	4809	0C40	007C	C0FC	IF RST THEN SKIP		06855C00 D
1558	4809	0C40	007C	C0FC	IF RST THEN SKIP		06856C00 D
1559	4809	0C40	007C	C0FC	IF RST THEN SKIP		06857C00 D
1560	4809	0C40	007C	C0FC	IF RST THEN SKIP		06858C00 D
1561	4809	0C40	007C	C0FC	IF RST THEN SKIP		06859C00 D
1562	4809	0C40	007C	C0FC	IF RST THEN SKIP		06860C00 D
1563	4809	0C40	007C	C0FC	IF RST THEN SKIP		06861C00 D
1564	4809	0C40	007C	C0FC	IF RST THEN SKIP		06862C00 D
1565	4809	0C40	007C	C0FC	IF RST THEN SKIP		06863C00 D
1566	4809	0C40	007C	C0FC	IF RST THEN SKIP		06864C00 D
1567	4809	0C40	007C	C0FC	IF RST THEN SKIP		06865C00 D
1568	4809	0C40	007C	C0FC	IF RST THEN SKIP		06866C00 D
1569	4809	0C40	007C	C0FC	IF RST THEN SKIP		06867C00 D
1570	4809	0C40	007C	C0FC	IF RST THEN SKIP		06868C00 D
1571	4809	0C40	007C	C0FC	IF RST THEN SKIP		06869C00 D
1572	4809	0C40	007C	C0FC	IF RST THEN SKIP		06870C00 D
1573	4809	0C40	007C	C0FC	IF RST THEN SKIP		06871C00 D
1574	4809	0C40	007C	C0FC	IF RST THEN SKIP		06872C00 D
1575	4809	0C40	007C	C0FC	IF RST THEN SKIP		06873C00 D
1576	4809	0C40	007C	C0FC	IF RST THEN SKIP		06874C00 D
1577	4809	0C40	007C	C0FC	IF RST THEN SKIP		06875C00 D
1578	4809	0C40	007C	C0FC	IF RST THEN SKIP		06876C00 D
1579	4809	0C40	007C	C0FC	IF RST THEN SKIP		06877C00 D
1580	4809	0C40	007C	C0FC	IF RST THEN SKIP		06878C00 D
1581	4809	0C40	007C	C0FC	IF RST THEN SKIP		06879C00 D
1582	4809	0C40	007C	C0FC	IF RST THEN SKIP		06880C00 D
1583	4809	0C40	007C	C0FC	IF RST THEN SKIP		06881C00 D
1584	4809	0C40	007C	C0FC	IF RST THEN SKIP		06882C00 D
1585	4809	0C40	007C	C0FC	IF RST THEN SKIP		06883C00 D
1586	4809	0C40	007C	C0FC	IF RST THEN SKIP		06884C00 D
1587	4809	0C40	007C	C0FC	IF RST THEN SKIP		06885C00 D
1588	4809	0C40	007C	C0FC	IF RST THEN SKIP		06886C00 D
1589	4809	0C40	007C	C0FC	IF RST THEN SKIP		06887C00 D
1590	4809	0C40	007C	C0FC	IF RST THEN SKIP		06888C00 D
1591	4809	0C40	007C	C0FC	IF RST THEN SKIP		06889C00 D
1592	4809	0C40	007C	C0FC	IF RST THEN SKIP		06890C00 D
1593	4809	0C40	007C	C0FC	IF RST THEN SKIP		06891C00 D
1594	4809	0C40	007C	C0FC	IF RST THEN SKIP		06892C00 D
1595	4809	0C40	007C	C0FC	IF RST THEN SKIP		06893C00 D
1596	4809	0C40	007C	C0FC	IF RST THEN SKIP		06894C00 D
1597	4809	0C40	007C	C0FC	IF RST THEN SKIP		06895C00 D
1598	4809	0C40	007C	C0FC	IF RST THEN SKIP		06896C00 D
1599	4809	0C40	007C	C0FC	IF RST THEN SKIP		06897C00 D
1600	4809	0C40	007C	C0FC	IF RST THEN SKIP		06898C00 D
1601	4809	0C40	007C	C0FC	IF RST THEN SKIP		06899C00 D
1602	4809	0C40	007C	C0FC	IF RST THEN SKIP		06900C00 D
1603	4809	0C40	007C	C0FC	IF RST THEN SKIP		06901C00 D
1604	4809	0C40	007C	C0FC	IF RST THEN SKIP		06902C00 D
1605	4809	0C40	007C	C0FC	IF RST THEN SKIP		06903C00 D
1606	4809	0C40	007C	C0FC	IF RST THEN SKIP		06904C00 D
1607	4809	0C40	007C	C0FC	IF RST THEN SKIP		06905C00 D
1608	4809	0C40	007C	C0FC	IF RST THEN SKIP		06906C00 D
1609	4809	0C40	007C	C0FC	IF RST THEN SKIP		06907C00 D
1610	4809	0C40	007C	C0FC	IF RST THEN SKIP		06908C00 D
1611	4809	0C40	007C	C0FC	IF RST THEN SKIP		06909C00 D
1612	4809	0C40	007C	C0FC	IF RST THEN SKIP		06910C00 D
1613	4809	0C40	007C	C0FC	IF RST THEN SKIP		06911C00 D
1614	4809	0C40	007C	C0FC	IF RST THEN SKIP		06912C00 D
1615	4809	0C40	007C	C0FC	IF RST THEN SKIP		06913C00 D
1616	4809	0C40	007C	C0FC	IF RST THEN SKIP		06914C00 D
1617	4809	0C40	007C	C0FC	IF RST THEN SKIP		06915C00 D
1618	4809	0C40	007C	C0FC	IF RST THEN SKIP		06916C00 D
1619	4809	0C40	007C	C0FC	IF RST THEN SKIP		06917C00 D
1620	4809	0C40	007C	C0FC	IF RST THEN SKIP		06918C00 D
1621	4809	0C40	007C	C0FC	IF RST THEN SKIP		06919C00 D
1622	4809	0C40	007C	C0FC	IF RST THEN SKIP		06920C00 D
1623	4809	0C40	007C				


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14E4 4809 A003 C030 C0F0      % CLEAR THE OLD PAR      06A36100 0
14E5 0000 0000 0000 0020      06A39100 0
14E6 4809 A001 40FF 00F0      06A4C100 0
14E7 4809 AC5C 4000 00F0      06B01C00 0
14E8 66EC 0000 0000 004C      06B02C00 0
                                     % NOT IMPLEMENTED      06B03C00 0
14E9 4E5C 0000 0070 0040      06B04C00 0
                                     % NOT IMPLEMENTED      06B05000 0
14EA 4E5C 0000 0070 0040      06B06C00 0
                                     % NOT IMPLEMENTED      06B07C00 0
14EB 4E50 0003 0030 004C      06B08C00 0
                                     % NOT IMPLEMENTED      06B09100 0
14EC 4E50 0000 0000 0040      06B0A000 0
                                     % NOT IMPLEMENTED      06B0B100 0
                                     % NOT IMPLEMENTED      06B0C100 0
                                     % NOT IMPLEMENTED      06B0D100 0
                                     % NOT IMPLEMENTED      06B0E100 0
                                     % NOT IMPLEMENTED      06B0F100 0
                                     % NOT IMPLEMENTED      06B10C00 0
                                     % NOT IMPLEMENTED      06B11C00 0
                                     % NOT IMPLEMENTED      06B12C00 0
                                     % NOT IMPLEMENTED      06B13C00 0
                                     % NOT IMPLEMENTED      06B14C00 0
                                     % NOT IMPLEMENTED      06B15C00 0
                                     % NOT IMPLEMENTED      06B16C00 0
                                     % NOT IMPLEMENTED      06B17C00 0
                                     % NOT IMPLEMENTED      06B18C00 0
                                     % NOT IMPLEMENTED      06B19C00 0
                                     % NOT IMPLEMENTED      06B1AC00 0
                                     % NOT IMPLEMENTED      06B1BC00 0
                                     % NOT IMPLEMENTED      06B1CC00 0
                                     % NOT IMPLEMENTED      06B1DC00 0
                                     % NOT IMPLEMENTED      06B1EC00 0
                                     % NOT IMPLEMENTED      06B1FC00 0
                                     % NOT IMPLEMENTED      06B20C00 0
                                     % NOT IMPLEMENTED      06B21C00 0
                                     % NOT IMPLEMENTED      06B22C00 0
                                     % NOT IMPLEMENTED      06B23C00 0
                                     % NOT IMPLEMENTED      06B24C00 0
                                     % NOT IMPLEMENTED      06B25C00 0
                                     % NOT IMPLEMENTED      06B26C00 0
                                     % NOT IMPLEMENTED      06B27C00 0
                                     % NOT IMPLEMENTED      06B28C00 0
                                     % NOT IMPLEMENTED      06B29C00 0
                                     % NOT IMPLEMENTED      06B2AC00 0
                                     % NOT IMPLEMENTED      06B2BC00 0
                                     % NOT IMPLEMENTED      06B2CC00 0
                                     % NOT IMPLEMENTED      06B2DC00 0
                                     % NOT IMPLEMENTED      06B2EC00 0
                                     % NOT IMPLEMENTED      06B2FC00 0
                                     % NOT IMPLEMENTED      06B30C00 0
                                     % NOT IMPLEMENTED      06B31C00 0
                                     % NOT IMPLEMENTED      06B32C00 0
                                     % NOT IMPLEMENTED      06B33C00 0
                                     % NOT IMPLEMENTED      06B34C00 0
                                     % NOT IMPLEMENTED      06B35C00 0
                                     % NOT IMPLEMENTED      06B36C00 0
                                     % NOT IMPLEMENTED      06B37C00 0
                                     % NOT IMPLEMENTED      06B38C00 0
                                     % NOT IMPLEMENTED      06B39C00 0
                                     % NOT IMPLEMENTED      06B3AC00 0
                                     % NOT IMPLEMENTED      06B3BC00 0
                                     % NOT IMPLEMENTED      06B3CC00 0
                                     % NOT IMPLEMENTED      06B3DC00 0
                                     % NOT IMPLEMENTED      06B3EC00 0
                                     % NOT IMPLEMENTED      06B3FC00 0
                                     % NOT IMPLEMENTED      06B40C00 0
                                     % NOT IMPLEMENTED      06B41C00 0
                                     % NOT IMPLEMENTED      06B42C00 0
                                     % NOT IMPLEMENTED      06B43C00 0
                                     % NOT IMPLEMENTED      06B44C00 0
                                     % NOT IMPLEMENTED      06B45C00 0
                                     % NOT IMPLEMENTED      06B46C00 0
                                     % NOT IMPLEMENTED      06B47C00 0
                                     % NOT IMPLEMENTED      06B48C00 0
                                     % NOT IMPLEMENTED      06B49C00 0
                                     % NOT IMPLEMENTED      06B4AC00 0
                                     % NOT IMPLEMENTED      06B4BC00 0
                                     % NOT IMPLEMENTED      06B4CC00 0
                                     % NOT IMPLEMENTED      06B4DC00 0
                                     % NOT IMPLEMENTED      06B4EC00 0
                                     % NOT IMPLEMENTED      06B4FC00 0
                                     % NOT IMPLEMENTED      06B50C00 0
                                     % NOT IMPLEMENTED      06B51C00 0
                                     % NOT IMPLEMENTED      06B52C00 0
                                     % NOT IMPLEMENTED      06B53C00 0
                                     % NOT IMPLEMENTED      06B54C00 0
                                     % NOT IMPLEMENTED      06B55C00 0
                                     % NOT IMPLEMENTED      06B56C00 0
                                     % NOT IMPLEMENTED      06B57C00 0
                                     % NOT IMPLEMENTED      06B58C00 0
                                     % NOT IMPLEMENTED      06B59C00 0
                                     % NOT IMPLEMENTED      06B5AC00 0
                                     % NOT IMPLEMENTED      06B5BC00 0
                                     % NOT IMPLEMENTED      06B5CC00 0
                                     % NOT IMPLEMENTED      06B5DC00 0
                                     % NOT IMPLEMENTED      06B5EC00 0
                                     % NOT IMPLEMENTED      06B5FC00 0
                                     % NOT IMPLEMENTED      06B60C00 0
                                     % NOT IMPLEMENTED      06B61C00 0
                                     % NOT IMPLEMENTED      06B62C00 0
                                     % NOT IMPLEMENTED      06B63C00 0
                                     % NOT IMPLEMENTED      06B64C00 0
                                     % NOT IMPLEMENTED      06B65C00 0
                                     % NOT IMPLEMENTED      06B66C00 0
                                     % NOT IMPLEMENTED      06B67C00 0
                                     % NOT IMPLEMENTED      06B68C00 0
                                     % NOT IMPLEMENTED      06B69C00 0
                                     % NOT IMPLEMENTED      06B6AC00 0
                                     % NOT IMPLEMENTED      06B6BC00 0
                                     % NOT IMPLEMENTED      06B6CC00 0
                                     % NOT IMPLEMENTED      06B6DC00 0
                                     % NOT IMPLEMENTED      06B6EC00 0
                                     % NOT IMPLEMENTED      06B6FC00 0
                                     % NOT IMPLEMENTED      06B70C00 0
                                     % NOT IMPLEMENTED      06B71C00 0
                                     % NOT IMPLEMENTED      06B72C00 0
                                     % NOT IMPLEMENTED      06B73C00 0
                                     % NOT IMPLEMENTED      06B74C00 0
                                     % NOT IMPLEMENTED      06B75C00 0
                                     % NOT IMPLEMENTED      06B76C00 0
                                     % NOT IMPLEMENTED      06B77C00 0
                                     % NOT IMPLEMENTED      06B78C00 0
                                     % NOT IMPLEMENTED      06B79C00 0
                                     % NOT IMPLEMENTED      06B7AC00 0
                                     % NOT IMPLEMENTED      06B7BC00 0
                                     % NOT IMPLEMENTED      06B7CC00 0
                                     % NOT IMPLEMENTED      06B7DC00 0
                                     % NOT IMPLEMENTED      06B7EC00 0
                                     % NOT IMPLEMENTED      06B7FC00 0
                                     % NOT IMPLEMENTED      06B80C00 0
                                     % NOT IMPLEMENTED      06B81C00 0
                                     % NOT IMPLEMENTED      06B82C00 0
                                     % NOT IMPLEMENTED      06B83C00 0
                                     % NOT IMPLEMENTED      06B84C00 0
                                     % NOT IMPLEMENTED      06B85C00 0
                                     % NOT IMPLEMENTED      06B86C00 0
                                     % NOT IMPLEMENTED      06B87C00 0
                                     % NOT IMPLEMENTED      06B88C00 0
                                     % NOT IMPLEMENTED      06B89C00 0
                                     % NOT IMPLEMENTED      06B8AC00 0
                                     % NOT IMPLEMENTED      06B8BC00 0
                                     % NOT IMPLEMENTED      06B8CC00 0
                                     % NOT IMPLEMENTED      06B8DC00 0
                                     % NOT IMPLEMENTED      06B8EC00 0
                                     % NOT IMPLEMENTED      06B8FC00 0
                                     % NOT IMPLEMENTED      06B90C00 0
                                     % NOT IMPLEMENTED      06B91C00 0
                                     % NOT IMPLEMENTED      06B92C00 0
                                     % NOT IMPLEMENTED      06B93C00 0
                                     % NOT IMPLEMENTED      06B94C00 0
                                     % NOT IMPLEMENTED      06B95C00 0
                                     % NOT IMPLEMENTED      06B96C00 0
                                     % NOT IMPLEMENTED      06B97C00 0
                                     % NOT IMPLEMENTED      06B98C00 0
                                     % NOT IMPLEMENTED      06B99C00 0
                                     % NOT IMPLEMENTED      06B9AC00 0
                                     % NOT IMPLEMENTED      06B9BC00 0
                                     % NOT IMPLEMENTED      06B9CC00 0
                                     % NOT IMPLEMENTED      06B9DC00 0
                                     % NOT IMPLEMENTED      06B9EC00 0
                                     % NOT IMPLEMENTED      06B9FC00 0
14ED 5F90 C0C3 0070 C06C      % LOAD ADDRESS REGISTER(S) 06A58C00 0
14EE 4809 C640 C740 00F0      06A59C00 0
14EF 1EBC 0073 C030 00C0      06A61C00 0
14F0 4809 C003 003C 00FC      06A62C00 0
14F1 4824 0000 0000 00F0      06A63C00 0
14F2 1ECC 00C0 0C00 0040      06A64C00 0
14F3 1E00 C003 0070 0040      06A65C00 0
14F4 3000 0C00 007C 0040      06A66C00 0
14F5 1E00 0000 0000 0040      06A67C00 0
14F6 4809 E155 0000 00F0      06A68C00 0
14F7 00FC C0C0 0000 C0C0      06A69C00 0
14F8 2100 0000 0000 006C      06A6AC00 0
14F9 4E50 0000 0000 0060      06A6BC00 0
14FA 4809 0C40 003C C0F0      06A6CC00 0
14FB 4809 E000 803C 00F0      06A6DC00 0
14FC 30F0 0C00 0C00 0080      06A6EC00 0
14FD 4809 2C56 C87C C0F0      06A6FC00 0
14FE 51C0 0003 007C 0060      06A70C00 0
14FF 2F3C 0003 003C C06C      06A71C00 0
1500 48C9 2C56 2030 00F0      06A72C00 0
1501 00FC C0C0 C0C0 00E0      06A73C00 0
1502 4809 C643 001C C0F0      06A74C00 0
1503 3000 0C00 000C 00C0      06A75C00 0
1504 4809 0000 007C 00F0      06A76C00 0
1505 2F50 0C00 003C C06C      06A77C00 0
1506 66EC C0C3 0C00 0040      06A78C00 0
1507 4809 E156 0000 C0F0      06A79C00 0
1508 00FC 0C00 C000 C06C      06A7AC00 0
1509 51C0 0C00 0000 0060      06A7BC00 0
150A 2100 C0C0 0070 0060      06A7CC00 0
150B 4809 0C41 003C C0F0      06A7DC00 0
150C 0000 C0C0 0070 C030      06A7EC00 0

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1598 4809 0C41 1000 00F0
1599 001C 0000 00F0 00F0
159A 4809 2F5C 801C 00F0
159B 2F30 00C0 00C0 00F0
159C 4809 EC5C 100C 00F0
159D 4809 CFC0 00C0 00F0
159E 49C9 E000 987C 00F0
159F 2000 0000 00C0 00F0
15A0 4809 E001 0820 00F0
15A1 0000 00C0 00C0 00F0
15A2 4809 0C40 303F 00F0
15A3 2F50 00C0 0000 00F0
15A4 4809 00C0 00F0 20F0
15A5 4809 0F43 801C 00F0
15A6 2F30 00C0 00C0 00F0
15A7 4809 00C0 00F0 00F0
15A8 0000 00C0 00C0 00F0
15A9 2F5C 00C0 0000 00F0
15AA 56E0 0003 0F2C 00F0

B L = A3
16 = SAR J 1 = LIT
LIT OR BHAR = HAR2
EINPUI - 1 = CPCK
A3 OR B = A3
A2 = SAR
A3 R = A3,BJ SET LC1
SETCCA - 1 = CPCK
A3 L = B
COMP 16 = SAR
B R = HIR
EINPUI - 1 = CPCK
ASR OR BHAR = HAR2
BHAR R = HAR2
B = SAR
A3 = HIR
A2 = SAR
EINPUI - 1 = CPCK
OPCODE - 1 = MPCK

07078100 D
07079000 D
07080100 D
07081200 D
07082300 D
07083400 D
07084500 D
07085600 D
07086700 D
07087800 D
07088900 D
07090000 D
07091100 D
07092200 D
07093300 D
07094400 D
07095500 D
07096600 D
07097700 D
07098800 D
07099900 D
07101000 D
07102100 D
07103200 D
07104300 D
07105400 D
07106500 D
07107600 D
07108700 D
07109800 D
07110900 D
07112000 D
07113100 D
07114200 D
07115300 D
07116400 D
07117500 D
07118600 D
07119700 D
07120800 D
07121900 D
07123000 D
07124100 D
07125200 D
07126300 D
07127400 D
07128500 D
07129600 D
07130700 D
07131800 D
07132900 D
07134000 D
07135100 D
07136200 D
07137300 D

% R(A+1)
% (R(A+1)) INTO B
% A3 = (R(A+1))/(R(A+1))
% 07083500 D
% 07084600 D
% 07085700 D
% 07086800 D
% 07087900 D
% 07089000 D
% 07090100 D
% 07091200 D
% 07092300 D
% 07093400 D
% 07094500 D
% 07095600 D
% 07096700 D
% 07097800 D
% 07098900 D
% 07100000 D
% 07101100 D
% 07102200 D
% 07103300 D
% 07104400 D
% 07105500 D
% 07106600 D
% 07107700 D
% 07108800 D
% 07109900 D
% 07111000 D
% 07112100 D
% 07113200 D
% 07114300 D
% 07115400 D
% 07116500 D
% 07117600 D
% 07118700 D
% 07119800 D
% 07120900 D
% 07122000 D
% 07123100 D
% 07124200 D
% 07125300 D
% 07126400 D
% 07127500 D
% 07128600 D
% 07129700 D
% 07130800 D
% 07131900 D
% 07133000 D
% 07134100 D
% 07135200 D
% 07136300 D
% 07137400 D

% RL TYPE ALG RIGHT DOUBLE SHIFT
% RIGHT SHIFT (R(A+1),R(A+1)) M (0-3)
% SIGN FILL AND SET CC
% ISOLATE *H* FIELD
% R(A) INTO HAR2
% TEMP STORAGE
% (R(A)) INTO B
% PUT B IN THE ADDER
% NEG SIGN FLAG
% A3 = (R(A+1))/(INSTRUCTION)
% (R(A+1)) INTO B
% CLEAR LHM OF A3
% A3 = (R(A+1))/(R(A+1))
% PERFORM SHIFT
% B = 1111/0000 OR B = 0000/0000
% SET THE (CONDITION BITS)
% (R(A+1)) SHIFTED INTO HIR
% REFERENCE 961
% R(A)

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07603:


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150F 30C0 00C0 0000 00C0      16 = SAR
1500 2F5C 0000 0000 00A0      OUTPUT - 1 = CPCR
1501 66EC 00C0 0000 00A0      OPCODE - 1 = MPCR

OPCODE61: XF0CODE - 1 = CPCR
A2 + AMPCR = AMPCR
0P61F - 1 = AMPCR
STEP
EXEC

1502 5F9C 00C0 0000 006C      OP610 - 1 = MPCR
1503 4809 C640 00C0 006C      A2 + AMPCR = AMPCR
1504 1F80 0F00 0000 00C0      0P61F - 1 = AMPCR
1505 4809 C0C0 0000 00C0      STEP
1506 4824 00C0 00C0 00C0      EXEC

1507 1F90 C000 0000 004C      OP610:
1508 1FAC 00C0 0000 004C
1509 1F0C 0F00 0000 0040
150A 1FCC 0F00 0000 0040

OP610:
150B 4809 2C56 20C0 00C0      LIT AND B = A2
150C 80C0 C0C0 00C0 0060      15 = LIT 4 = SAR
150D 4809 C0C0 8000 00C0      B R = B
150E 4809 2C56 0800 00C0      REGSTACK - 1 = CPCR
150F 51C0 0F00 00C0 00A0      INPUT - 1 = CPCR
1510 2F3C 0F00 0000 0060      NOT A2 = A2
1511 4809 C0C0 20C0 00C0      A2 + 1 = SAR
1512 4809 C0C0 00C0 00C0      B L = B
1513 4809 0C41 00C0 00C0      B R = A2
1514 4809 C0C0 00C0 00C0      16 = SAR
1515 00C0 0000 0000 0020      NOT A2
1516 4809 C0C0 00C0 00C0      IF NOT A2 THEN SET LCI
1517 63C9 00C0 00C0 00C0      OVBIT - 1 = CPCR
1518 5020 00C0 00C0 0060      B L = B
1519 4809 0C41 00C0 00C0      COMP 16 = SAR
151A 0000 0000 0000 0020      P R = M1R, B
151B 4809 0C40 00C0 00C0      INPUT - 1 = CPCR
151C 2F5C 00C0 00C0 0060      SETCCA - 1 = CPCR
151D 20C0 0000 0000 00A0      OPCODE - 1 = MPCR
151E 50E0 00C0 00C0 00A0

OP611:
151F 4809 2C56 20C0 00C0      LIT AND P = A2
1520 80C0 C0C0 00C0 00C0      15 = LIT 4 = SAR
1521 4809 0C40 80C0 00C0      P R = B
1522 4809 2C56 0800 00C0      REGSTACK - 1 = CPCR
1523 51C0 00C0 00C0 0060      INPUT - 1 = CPCR
1524 2F3C 0F00 0000 0060      B = A3
1525 4809 0C40 1C00 00C0      A3 L = A3
1526 4809 E0C1 10C0 C0C0      COMP 16 = SAR
1527 0100 0000 0000 00A0      A3 OR B = A3
1528 4809 EC5C 10C0 00C0      A2 = B
1529 4809 C000 7000 00C0      LIT - B = A2
1530 4809 2C56 20C0 00C0      A2 = SAR
1531 4809 C000 0000 00C0      A3 C = A3
1532 4809 E0C1 90C0 00C0      COMP 16 = SAR
1533 00C0 0F00 00C0 0020

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1632 1809 C0C0 0C30 80F0
1633 19C9 E001 9830 C0F0
1634 20C0 0000 0C9C 006C
1635 1809 E001 0830 00F0
1636 0000 0000 0000 C020
1637 1809 0C40 8C30 C0F0
1638 2F50 00C0 0C9C 006C
1639 4809 0000 0C9C 20F0
163A 4809 6F43 801C 00F0
163B 00C0 C0C0 0C30 0010
163C 1809 E000 803C 00FC
163D 0000 00C0 C030 0020
163E 2F5C C00C 0C9C C060
163F 56E0 00C0 0C30 004C

1640 5C9C C0C0 0030 0060
1641 4809 C643 0C30 00F0
1642 1F0C 00C0 C030 00F0
1643 4809 0000 0C3C 00FC
1644 4824 C000 0C30 0010

1645 1FEC 0000 007C C090
1646 1FEC 0003 0C30 004C
1647 200C 00F0 001C 004C
1648 2010 00C0 0C30 004C

1649 228C C0C0 0C9C C060
164A 4809 C641 2C3C 00FC
164B 00F0 0C3C 007C 00A0
164C 4839 E156 0830 C0F0
164D 4809 0C41 0C30 C0F0
164E 4849 CC5E 0C30 00FC
164F 78C9 0000 C03C 00FC
1650 1E70 C0C0 0C30 006C
1651 4F1C 0C3C CC9C 0060
1652 4809 00C0 003C 00FC
1653 4809 0C40 5B3C 00F0
1654 00C0 00C0 0C3C C02C
1655 200C 00C0 0C3C 0060
1656 2F5C C0C0 003C 004C
1657 56EC 00C0 007C C04C

1658 4809 2C5C 0C30 00F0
1659 9CFC 0C3C 0C30 0080
165A 4809 0C40 8B3C 00FC
165B 4809 2C5C 083C 00F0
165C 51EC C0C0 0C3C C060
165D 4809 0F41 0C30 C0F0
165E 000C 0C30 0C30 0030
165F 2F3C C0C0 0C30 0060
1660 4809 0C41 2C00 C0F0
1661 001C 0C3C 0C30 00A0

A2 + 1 = SAR
A3 C = A340J SET LC1
SETCCA - 1 = CPCR
A3 L = B
COMP 16 = SAR
B R = MIR
[OUTPUT] - 1 = CPCR
ASR
RHAR R = HAR2
B = SAR
A3 R = MIR
16 = SAR
E0UTPUT - 1 = CPCR
OPCODE - 1 = MPCR

OPCODE62: XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP62F - 1 = AMPCR
STEP
EXEC

OP62F1
OP620 - 1 = MPCR
OP621 - 1 = MPCR
OP622 - 1 = MPCR
OP623 - 1 = MPCR

OP620:
CONTENTSNA - 1 = CPCR
E L = A2
COMP 16 = SAP; 15 = LIT
A3 AND LIT = B
B L = B
A2 - B = MIR; SET LC2
IF A0V THEN SET LC1
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
RMI
B R = MIR#B
16 = SAR
SETCCA - 1 = CPCR
E0UTPUT - 1 = CPCR
OPCODE - 1 = MPCR

OP621:
LIT AND B = MIR
15 = LIT; B = SAR
B R = R
LIT AND B = 0
REGSTACK - 1 = CPCR
RHAR L = BR1
COMP B = SAR
FINPUT - 1 = CPCR
B L = A2
CMP 16 = SAR; 1 = LIT

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1695 1E70 0000 007C 0060
1696 4E10 0000 0070 0060
1697 49C9 10C3 0070 0060
1698 2000 00C3 007C 0060
1699 4809 0000 0000 0060
169A 4809 00C4 2030 0060
169B 0000 00C4 0000 0060
169C 4809 0C40 8070 0060
169D 4809 0C00 8C30 0060
169E 2F50 0000 0000 0060
169F 4809 0000 0000 0060
16A0 4809 0F43 8C1C 0060
16A1 0000 0000 0000 0060
16A2 4809 0C40 0000 0060
16A3 2F50 0C03 0000 0060
16A4 66EC 0000 0000 0060

16A5 5F90 0000 0000 0060
16A6 4809 0C40 0000 0060
16A7 202C 0000 0000 0060
16A8 4809 0000 0000 0060
16A9 4824 0000 0070 0060
16AA 2030 0000 0070 0060
16AB 2080 0000 0000 0060
16AC 205C 00C3 0070 0060
16AD 2060 0000 0070 0060

16AE 4809 2C56 0B0C 0060
16AF 0F0C 0000 0000 0060
16B0 4809 0C40 0000 0060
16B1 4809 0C00 0000 0060
16B2 4809 2C56 0E30 0060
16B3 51CC 0000 0000 0060
16B4 2F50 0000 0000 0060
16B5 2180 0000 0000 0060
16B6 66EC 0000 0000 0060

16B7 4809 2C56 0B00 0060
16B8 0F0C 0000 0000 0060
16B9 4809 0000 0000 0060
16BA 228C 10C3 0000 0060
16BB 4809 0C43 2030 0060
16BC 0000 0000 0000 0060
16BD 4809 0C43 2E70 0060
16BE 20C0 0000 0000 0060
16BF 4849 0C5E 0C30 0060
16C0 78C9 0C00 0000 0060
16C1 1E70 0000 0000 0060
16C2 4F1C 0000 0000 0060
16C3 66EC 0000 0000 0060

CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
BML1 SET LC1
SETCCA - 1 = CPCR
B*1
B L = A2
CDMP 16 = SAR
R R = B
A2 R = MIR
ASR
DMAR R = MAR2
B = SAR
FOUIPUT - 1 = CPCR
FOUIPUT - 1 = MPCK
OPCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP63F - 1 = AMPCR
STEP
EXEC
OP63F:
OP630 - 1 = MPCK
OP631 - 1 = MPCK
OP632 - 1 = MPCK
OP633 - 1 = MPCK

OP630:
LIT AND B = B
15 = LITI 4 = SAR
P = MIR
A3 R = B
LIT AND E = B
REGSTACK - 1 = CPCR
FOUIPUT - 1 = CPCR
SET00 - 1 = CPCR
OPCODE - 1 = MPCK

OP631:
LIT AND B = MIR
15 = LITI
A3 = B
CONTENTSRA - 1 = CPCR
B L = A2, BML
CDMP 16 = SAR
B L = B
SETCC - 1 = CPCR
A2 - B = MIR; SET LC2
IF ADV THEN SET LC1
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
OPCODE - 1 = MPCK

CARRY - 1 = CPCR
BML1 SET LC1
SETCCA - 1 = CPCR
B*1
CDMP 16 = SAR
R R = B
A2 R = MIR
ASR
DMAR R = MAR2
B = SAR
FOUIPUT - 1 = CPCR
FOUIPUT - 1 = MPCK
OPCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP63F - 1 = AMPCR
STEP
EXEC
OP63F:
OP630 - 1 = MPCK
OP631 - 1 = MPCK
OP632 - 1 = MPCK
OP633 - 1 = MPCK

OP630:
LIT AND B = B
15 = LITI 4 = SAR
P = MIR
A3 R = B
LIT AND E = B
REGSTACK - 1 = CPCR
FOUIPUT - 1 = CPCR
SET00 - 1 = CPCR
OPCODE - 1 = MPCK

OP631:
LIT AND B = MIR
15 = LITI
A3 = B
CONTENTSRA - 1 = CPCR
B L = A2, BML
CDMP 16 = SAR
B L = B
SETCC - 1 = CPCR
A2 - B = MIR; SET LC2
IF ADV THEN SET LC1
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
OPCODE - 1 = MPCK

```



```

14C4 2809 0C40 8030 C0FC
14C5 9CFC 0C00 CF70 00B0
14C6 9809 2C56 0000 C0F0
14C7 51C0 0C00 0000 C060
14C8 4809 CF41 CF70 00FC
14C9 0000 0000 0000 0030
14CA 4809 0F45 0B30 C0FC
14CB 51C0 0C00 0030 C060
14CC 2F30 00C0 CC70 C060
14CD 4809 E155 2000 00F0
14CE G0FC 0000 0000 00E0
14CF 4C60 0000 0030 C060
14D0 4809 0F00 0B30 00F0
14D1 2000 C000 0000 C060
14D2 4809 EC01 0B30 00F0
14D3 00C0 0000 CC70 C020
14D4 4809 CC40 8630 C0FC
14D5 2F50 C0C0 CC70 0060
14D6 4809 0C00 0000 00F0
14D7 4809 0F43 861C 00F0
14D8 0000 00C0 0000 0010
14D9 4809 0F00 8630 00F0
14DA 0000 0000 0030 0020
14DB 2F50 C0C0 0000 C06C
14DC 5650 0000 0030 C040

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```

% TYPE RL LITERAL MULTIPLY
% R(A+1) X M = (R(A)*R(A+1)), SET CC

B R = B; IF LCI
4 = SARI 15 = LII
LII AND B = B
REGSTACK - 1 = CPGR
PHAR L = BR1
COMP 8 = SAR
BHAR + 1 = B
REGSTACK - 1 = CHCR
EINPUT - 1 = CPGR
A3 AND LII = A2
15 = LIT
MULT - 1 = CPGR
A3 = B; MIR
SEITCCA - 1 = CPGR
A3 L = B
COMP 16 = SAR
B R = MIR
EINPUT - 1 = CPGR
ASR
BHAR R = HAR2
8 = SAR
A3 R = MIR
16 = SAR
EINPUT - 1 = CPGR
OPCODE - 1 = HPGR

% TYPE RL LITERAL DIVIDE
% (R(A)*R(A+1))/H = R(A+1), REMAINDER
% INTO R(A) SET CC AND OV
% ISOLATE "H"

LII AND 0 = B
15 = LIT; COMP 16 = SAR
B L = MIR
A3 R = R
4 = SAR
LII AND 0 = E
REGSTACK - 1 = CPGR
BHAR L = UR1
COMP 8 = SAR
EINPUT - 1 = CPGR
R L = A2
COMP 16 = SAR
BHAR + 1 = B
REGSTACK - 1 = CPGR
EINPUT - 1 = CPGR
A2 OR B = A2; BHI; SET LCI
A3 - 1 = CPGR
PHAR R = HAR2
8 = SAR
A2 = MIR
EINPUT - 1 = CPGR
A3 = B; MIR
BHAR + 1 = B
REGSTACK - 1 = CPGR
SEITCCA - 1 = CPGR
EINPUT - 1 = CPGR
CLEAROV - 1 = CPGR

```

```

14DD 4809 2C55 0B00 C0AC
14DE 00FC C0C0 0C7C 00AC
14DF 48C9 0C41 0C50 00F0
14E0 4809 0C00 8630 00FC
14E1 500C 0C00 0030 00C0
14E2 4809 2C56 CB40 C0F0
14E3 51C0 C000 0000 C06C
14E4 4809 0F41 0C20 00F0
14E5 0000 00C0 0000 0030
14E6 2F30 C0C0 0000 0060
14E7 48C9 CC41 207C 00F0
14E8 00C0 C0C0 0000 C02C
14E9 48C9 0F46 C030 C0FC
14EA 51C0 C000 0000 C060
14EB 2F50 C000 0000 C06C
14EC 0000 0000 0000 0000
14ED 2400 0000 0000 0000
14EE 4809 0000 0030 C0F0
14EF 4809 0F43 861C 00F0
14F0 0000 C0C0 0000 0010
14F1 4809 C000 0F40 00FC
14F2 2F50 C0C0 0000 0060
14F3 4809 EC00 0B30 00FC
14F4 2000 0000 0000 C060
14F5 4809 0F45 0B30 00F0
14F6 51C0 C000 0030 C060
14F7 2F50 C0C0 C030 C060
14F8 5050 0000 C000 C06C

```


248


```

178E 238C 60C0 C000 006C 07678C00 0
1790 4809 0C46 0C30 00F0 07679C00 C
1791 2F5C 00C3 003C 0060 07681C00 D
1792 66E0 0003 0000 0040 07683C00 D
1793 48C9 0C41 0B0C 00FC 07684C00 D
1794 00FC 0C0C 0C0C 0030 07685C00 D
1795 4809 0C40 9B3C 00F0 07686C00 D
1796 788C 0C03 0C0C 0050 07687C0C D
1797 4E5C 0C00 0000 004C 07688C0C C
1798 4E5C 00C3 0000 0040 076C9C00 D
1799 4E50 00C0 0C0C 0040 07691C00 D
179A 4E50 0C0C 003C 0040 07692C00 D
179B 4E50 00C0 000C 004C 07693C00 D
179C 4E50 0C0C 003C 0040 07694C00 D
179D 4E50 00C0 0000 004C 07695C00 D
179E 300C 0C00 0C0C 0040 07696C00 D
179F 0000 00C0 000C 0050 07697C00 D
17A0 792C 0C00 000C 005C 07698C00 D
17A1 777C 0000 0000 005C 07699C00 D
17A2 773C 00C3 0000 0000 07701C00 D
17A3 76AC 00C0 0000 005C 07703C00 C
17A4 752C 0C03 0000 005C 07704C00 D
17A5 74EC 0000 000C 000C 07705C00 D
17A6 73AC 0003 000C 005C 07706C0C D
17A7 726C 0000 0C3C 0050 07707C00 D
17A8 710C 00C3 0000 0050 07708C00 D
17A9 702C 00C3 003C 0050 07709C00 D
17AA 6FE0 0003 000C 000C 07711C00 C
17AB 50CC 00C0 0C3C 0050 07711C00 C
17AC 6C3C 0C03 0C00 0050 07711C00 C
17AD 5B6C 00C3 0C00 0050 07712C00 D
17AE 6A0C 0000 0C30 0050 07712C00 D
17AF 6A9C 0C03 0C0C 0000 07712C00 D
17B0 6850 00C3 0000 0C50 07712C00 D
17B1 576C 00C0 0000 0050 07712C00 D
17B2 6570 0003 0C30 0050 07712C00 D
17B3 648C 0C00 0000 0050 07712C00 D
17B4 644C 0C03 0000 0000 07712C00 D
17B5 623C 0C0C 000C 0050 07712C00 D
17B6 6020 0003 0C0C 0050 07712C00 D
17B7 5EEC 00C0 0000 0050 07712C00 D

```


1507 50A0 0000 00C0 005C
1504 5060 0000 0090 0000
1573 5AA0 0000 0030 0050
1572 56F0 0000 0000 0050
1571 5790 0000 0000 0050
1560 56F0 0000 0000 0000
1550 52E0 0000 0000 0050
1549 52E0 0000 0000 0050
1524 5200 0000 0000 0050
1527 5290 0000 0000 0000
14F5 50F0 0000 0000 0050
14F3 5060 0000 0000 0050
14F2 4F50 0000 0000 0050
14EF 4F10 0000 0000 0050
1492 4040 0000 0000 0050
1481 4C50 0000 0000 0050
1480 40E0 0000 0000 0050
14AF 4820 0000 0000 0050
14AC 4AEC 0000 0000 0000
1470 4950 0000 0000 0050
146F 4820 0000 0000 0050
146E 47C0 0000 0000 0050
146D 47C0 0000 0000 0050
146A 46C0 0000 0000 0000
1456 4560 0000 0000 0050
1455 4450 0000 0000 0050
1450 4000 0000 0000 0050
1431 4320 0000 0000 0050
1430 4320 0000 0000 0050
13FF 41FC 0000 0000 0050
13FE 40EC 0000 0000 0050
13FD 4090 0000 0000 0050
13FC 3FF0 0000 0000 0050
13F9 3F80 0000 0000 0000
1392 3E60 0000 0000 0050
1391 3000 0000 0000 0050
1390 3020 0000 0000 0050
13AC 3AEC 0000 0000 0000
1271 3960 0000 0000 0050
1270 3800 0000 0000 0050
136E 3710 0000 0000 0050
136B 36D0 0000 0000 0000
1328 3530 0000 0000 0050
132A 33D0 0000 0000 0050
1329 3380 0000 0000 0050
1328 32B0 0000 0000 0050
1225 1270 0000 0000 0000
12FA 3180 0000 0000 0050
12F7 3050 0000 0000 0050
12F6 2EAC 0000 0000 0050
1274 2F40 0000 0000 0050
1271 2F40 0000 0000 0050
12FE 2F40 0000 0000 0050
12E8 2F40 0000 0000 0050
12E5 2F40 0000 0000 0050
12E0 2F40 0000 0000 0050
12D0 2F40 0000 0000 0050
120C 2F40 0000 0000 0050
1207 2F40 0000 0000 0050

0120 F300 0000 0000 0040
 012A F20C 0000 0000 00C0
 01DE F15C 0000 0000 0040
 01DD F10C 0000 0000 0040
 01DC F0CC 0000 0000 004C
 01D0 F0EC 0000 0000 0040
 01D8 EDAE 0000 0000 00C0
 015E EAD0 0000 0000 004C
 015C E85F 0000 0000 0040
 0150 E5E9 0000 0000 004C
 0158 E5A0 0000 0000 00C0
 0100 E410 0000 0000 0040
 01FF E270 0000 0000 004C
 01FE E120 0000 0000 004C
 00FD E00C 0000 0000 0040
 00FA DFC0 0000 0000 00C0
 0079 DC0C 0000 0000 004C
 0077 D41C 0000 0000 004C
 0076 D79C 0000 0000 004C
 0073 D75C 0000 0000 00C0
 0019 D5C0 0000 0000 004C
 0018 D42C 0000 0000 004C
 0017 D280 0000 0000 004C
 0015 D15C 0000 0000 004C
 0013 D04C 0000 0000 00C0
 00BF D04C 0000 0000 0040
 00BE D230 0000 0000 0040
 00BD 2000 0000 0000 0040
 00BC 29F0 0000 0000 0040
 00B9 C8B8 0000 0000 00C0
 0032 C900 0000 0000 0040
 0031 C710 0000 0000 0040
 0030 C560 0000 0000 0040
 002F C320 0000 0000 0040
 002C C2EC 0000 0000 00C0
 00D5 C100 0000 0000 0040
 00D4 BF9C 0000 0000 004C
 00D3 BE9C 0000 0000 0040
 01D2 D05C 0000 0000 004C
 00CF D010 0000 0000 00C0
 00BC DC6C 0000 0000 00C0
 0027 DA30 0000 0000 0040
 0026 D70C 0000 0000 0040
 0024 D64C 0000 0000 0040
 0023 D82C 0000 0000 0040
 0061 D64C 0000 0000 0040
 005E D60C 0000 0000 0040
 00E9 D38C 0000 0000 0040
 00E8 D0C0 0000 0000 004C
 00E6 AE9F 0000 0000 0040
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 0071 AA3C 0000 0000 0040
 0070 A91C 0000 0000 0040
 006F A72C 0000 0000 0040
 006C A66C 0000 0000 00C0
 001F A5DF 0000 0000 004C
 001E A3DC 0000 0000 0040
 001D A360 0000 0000 0040
 001C A1F0 0000 0000 0040

0A19 A19C 00C0 0000 00C0
 0A00 A120 00C0 0070 0040
 0A05 A000 00C0 0070 0040
 0900 9F8C 00C0 0070 0040
 090C 9E7C 0000 0000 0040
 090A 9D00 00C0 0070 0040
 0907 9D90 00C0 0070 0040
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 0980 902C 00C0 0030 0040
 0989 9A4C 00C0 0030 0040
 0938 9880 00C0 0000 0040
 0935 987C 00C0 0000 0040
 0962 97FC 00C0 0030 0040
 0960 970C 0000 0000 0040
 095F 9620 0000 0000 0040
 095C 95EC 0000 0000 0040
 0934 9570 0000 0030 0040
 0932 9420 0000 0030 0040
 0931 9340 00C0 0000 0040
 092E 930C 0000 0030 0040
 092C 90F0 00C0 0000 0040
 0909 90EC 00C0 0000 0040
 0900 90EC 00C0 0000 0040
 08FE 90F0 00C0 0030 0040
 08A7 8A8C 00C0 0030 0040
 08AE 8ECC 00C0 0000 0040
 0880 80B0 00C0 0000 0040
 088C 9C8C 00C0 0000 0040
 0888 88EC 00C0 0030 0040
 088A 88A0 0000 0030 0040
 0830 916C 0000 0000 0040
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 067A 37CC 00C0 0030 0040
 07FF 8420 0000 0070 0040
 07EE 82CC 00C0 0030 0040
 07FD 822C 0000 0000 0040
 07FB 812C 00C0 0030 0040
 07FA 809C 00C0 0000 0040
 07E9 7FEC 00C0 0030 0040
 07E3 7180 00C0 0070 0040
 07EE 951C 0000 0030 0040
 07EC 7EFC 00C0 0030 0040
 07E9 7E80 0000 0000 0040
 07E7 777C 00C0 0000 0040
 07E5 777C 00C0 0000 0040
 073E 700C 00C0 0000 0040
 0730 7C30 00C0 0070 0040
 073C 7E60 0000 0030 0040
 0738 7A90 00C0 0000 0040
 0739 7A3C 00C0 0000 0040
 0738 7880 00C0 0030 0040
 0737 77F0 00C0 0030 0040
 0735 7500 00C0 0030 0040
 0734 74F0 00C0 0000 0040
 0733 73E0 0000 0030 0040
 0720 7320 0000 0000 0040
 0724 7E3C 00C0 0000 0040
 0722 700C 00C0 0000 0040
 0721 7240 00C0 0030 0040
 071E 720C 0000 0070 0040

[illegible]

046F 46F0 6703 0020 0040
 0460 5100 0000 0000 0060
 0469 46F0 0000 0000 0040
 0467 5100 0000 0000 0060
 0464 46F0 0000 0000 0040
 0462 5100 0000 0000 0060
 0460 46F0 0000 0000 0040
 045F 5100 0000 0000 0060
 045E 46F0 0000 0000 0040
 045D 5100 0000 0000 0060
 045B 46F0 0000 0000 0040
 0457 46F0 0000 0000 0060
 0456 46F0 0000 0000 0040
 0455 46F0 0000 0000 0060
 0452 46F0 0000 0000 0040
 044A 50E0 0000 0000 0060
 0444 4440 0000 0000 0040
 0442 5100 0000 0000 0060
 043E 4440 0000 0000 0040
 043C 4440 0000 0000 0060
 043A 5100 0000 0000 0040
 0436 50E0 0000 0000 0060
 0431 4300 0000 0000 0040
 0430 4300 0000 0000 0060
 042F 4370 0000 0000 0040
 042E 4310 0000 0000 0060
 042B 4200 0000 0000 0040
 0425 4400 0000 0000 0060
 0424 4250 0000 0000 0040
 041E 4400 0000 0000 0060
 041C 4400 0000 0000 0040
 0415 6330 0000 0000 0060
 0410 4140 0000 0000 0040
 0406 6330 0000 0000 0060
 03F0 66E0 0000 0000 0040
 03E3 3F70 0000 0000 0060
 03D5 66E0 0000 0000 0040
 02C8 3F70 0000 0000 0060
 03BE 4E50 0000 0000 0040
 03BD 30C0 0000 0000 0060
 039C 3DE0 0000 0000 0040
 03B9 3BE0 0000 0000 0060
 03AC 66E0 0000 0000 0040
 03A2 3F70 0000 0000 0060
 038E 66E0 0000 0000 0040
 0383 3F70 0000 0000 0060
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 0375 3990 0000 0000 0060
 0374 3F60 0000 0000 0040
 0371 3730 0000 0000 0060
 035E 3620 0000 0000 0040
 0357 34E0 0000 0000 0060
 0353 34E0 0000 0000 0040
 0348 61E0 0000 0000 0060
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 0310 61E0 0000 0000 0060
 0314 60E0 0000 0000 0040
 030F 60E0 0000 0000 0060
 0305 50FC 0000 0000 0040
 0301 5800 0000 0000 0060
 02F0 2F30 0000 0000 0060
 02EC 2F30 0000 0000 0040

CC5C	0830	00C0	007C	0040		
CC66	081C	0000	0000	0060		
CC58	097C	00C0	0070	006C		
CC5A	087C	00C3	0070	0060		
CC59	050C	00C0	007C	0040		
CC51	5CFC	00C0	0070	0040		
CC50	081C	00C0	007C	0060		
CC49	051C	00C0	007C	0060		
CC46	05EC	00C3	007C	0040		
CC42	051C	00C0	007C	0060		
CC41	0460	00C0	0070	0060		
CC36	060C	0000	007C	004C		
CC35	1540	0000	0070	004C		
CC32	1000	00C0	007C	0040		
CC2F	181C	00C7	007C	0040		
CC2C	187C	00C0	0070	0040		
CC29	1A4C	00C0	0070	004C		
CC26	162C	00C0	007C	004C		
CC23	1790	00C0	007C	004C		
CC20	036C	00C0	0070	0040		
CC1D	08F0	0000	007C	0040		
CC1A	048C	0000	007C	0040		
CC14	0A8C	0000	007C	0040		
CC11	1000	00C0	007C	0040		
CC0A	096C	0000	007C	0040		
CC07	06C0	0000	007C	0040		

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BIBLIOGRAPHY

1. Air Force Avionics Lab, Wright-Patterson AFB, Ohio, AFAL-TR-74-180, A Stack Machine Emulation, Anderson, C. M., January 1975.
2. Agrawala, A. K. and Rausher, T. G., "Microprogramming: Perspective and Status," IEEE Trans, C23, p. 817-37, August 1974.
3. Burkhard, W. A., "Flexible Computer Architectures for Research and Development," Computer Conference, Fall 1976.
4. Burroughs Corporation Report 64116, Emulation Facility, by Advanced Design Organization, Paoli, Pa., 28 June 1971.
5. Burroughs Corporation Report TR70-2, The Interpreter, by R. L. Davis, 16 February 1970.
6. Burroughs Corporation Report TR70-8, Microprogramming Manual for the Interpreter Based Systems, by Advanced Design Organization, Paoli, Pa., November 1970.
7. Burroughs Corporation Report 66143, Algol Reference Manual for the Interpreter Based System, by Advanced Design Organization, Paoli, Pa., 15 June 1975.
8. Computer Sciences Corporation, A Cost-Effective Emulation Approach for U. S. Army Telecommunications, by J. W. Carroll, p. 1-13.
9. Naval Electronics Laboratory Center and M. I. T. Sloan School of Management, Facilities Orientation Report, Volume 1, A Survey of the Navy Tactical Computer Applications and Executives, by Professors S. E. Madnick and J. D. Detreville, October 1975.

10. Haggerty, J. M. and Hartling, J. M., Emulation of the AN/UYK-7 Tactical Data Computer on the Burroughs D-Machine, Masters Thesis, Naval Postgraduate School, Monterey, California, December 1976.
11. Husson, S. S., Microprogramming: Principles and Practices, Prentice-Hall, Inc., 1970.
12. Jones, L., "Instruction Sequencing in Microprogrammed Computers," Proceedings NCC, 44, p. 91-8, 1975.
13. Lichstein, H. A., "When Should You Emulate?," Datamation, 15, p. 205-10, November 1969.
14. Mallach, E. G., "Emulator Architecture," Computer, p. 24-32, August 1975.
15. Mercer, R. J., "Microprogramming," Journal for the Association of Computing Machines, 4, p. 157-71, April 1957.
16. Naval Material Command UNCLASSIFIED Letter MAT 09Y:JER Serial 130 to Naval Electronic Systems Command, Subject: Standard Shipboard Tactical Digital Processors and Program Languages, 29 May 1973.
17. Reigel, E. W., Faber, U., and Fisher, D. A., "The interpreter - A microprogramming building block system," Proceedings SJCC, 40, p. 705-23, 1972.
18. Rosin, R. F., "Contemporary Concepts of Microprogramming and Emulation," Computer Surveys, 1, p. 197-212, December 1969.
19. Saal, H. J. and Schuster, L. J., On Measuring Computer Systems by Microprogramming.
20. Sperry Rand, UNIVAC, Computer Set AN/UYK20 Technical Manual Operations and Maintenance with Parts List, N 00039-73-C-0432, September 1974.
21. Sperry Rand, UNIVAC, AN/UYK-20 Computer Repertoire of Instructions, Fall 1976.

22. Sperry Rand, UNIVAC, AN/UYK-20 Technical Description, November 1976.
23. Sperry Rand, UNIVAC, User's Handbook for AN/UYK-20(V) Computer Volume 3 (Change 4), NAVELEX 0967-LP-598-2030, April 1976.
24. Wilkes, M. B., "The Growth of Interest in Microprogramming: A Literature Survey," Computer Surveys, 1, p. 139-45, September 1969.

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computer on the Bur-
roughs D-machine.

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